Aula 9

Engenharia de Sistemas Embarcados

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Tópico: Arquitetura ARM (MCB2300)

ARM7 NXP LPC2368

128/256/512-KB ISP/IAP 128-b wide FLASH	E-ICE/RTM interface embedded trace macrocell
16- to 40-KB SRAM	Enhanced vectored interrupt controller
16-/32-bit ARM7TDMI-S core	
Power management, Watchdog timer, internal RC, PLL	
10/100 Ethernet MAC with 16-KB SRAM	CAN 0, 1
USB 2.0 full-speed device with PHY, DMA, and 4-KB RAM FIFO	General-purpose DMA controller
8-channel/10-bit A/D converter	1-channel/10-bit D/A converter
Capture/compare timer 0, 1, 2, 3	PWM 0, 1
UART 0, 2, 3 UART 1 with modem control	SD/MMC card interface
PS	PC 0, 1, 2
SSP 0, 1 SPI 0	RTC with 2-KB battery RAM
I/O Ports (70) (104 for LPC2378)	

Key Features:

- 32-Bit ARM7® Core Architecture
- 72MHz operation (64 Dhrystone MIPs)
- Up to 512kB on-chip Flash and 58kB SRAM
- Ethernet 10/100 MAC with DMA
- USB 2.0 full-speed device with PHY and DMA
- CAN 2.0B with two channels
- General-purpose DMA controller
- I^2S, three I^2C, three SPI/SSP, and four UARTs
- 4MHz internal RC (IRC) oscillator trimmed to 1% accuracy

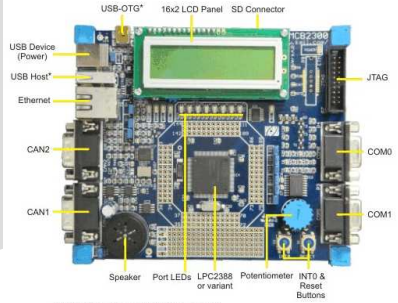
Aplicações

Applications

- Industrial control
- Medical systems
- Protocol converter
- Communications

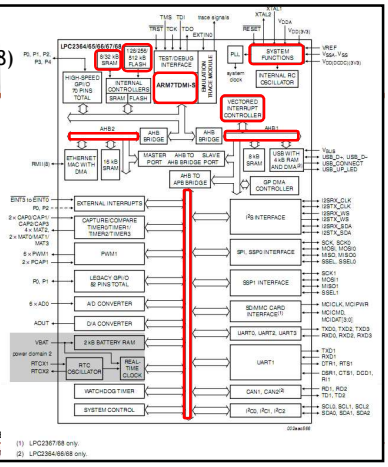
Type number	Flash (kB)	SRAM (kB)					Ethernet	USB device + 4 kB FIFO	SD/MMC	GP DMA	Channels		
		Local bus	Ethernet buffers	GP/USB	RTC	Total					CAN	ADC	DAC
LPC2364FBD100	128	8	16	8	2	34	RMII	yes	no	yes	2	6	1
LPC2364HBD100	128	8	16	8	2	34	RMII	yes	no	yes	2	6	1
LPC2364FET100	128	8	16	8	2	34	RMII	yes	no	yes	2	6	1
LPC2365FBD100	256	32	16	8	2	58	RMII	no	no	yes	-	6	1
LPC2366FBD100	256	32	16	8	2	58	RMII	yes	no	yes	2	6	1
LPC2367FBD100	512	32	16	8	2	58	RMII	no	yes	yes	-	6	1
LPC2368FBD100	512	32	16	8	2	58	RMII	yes	yes	yes	2	6	1
LPC2368FET100	512	32	16	8	2	58	RMII	yes	yes	yes	2	6	1

ARM7 MCB2300



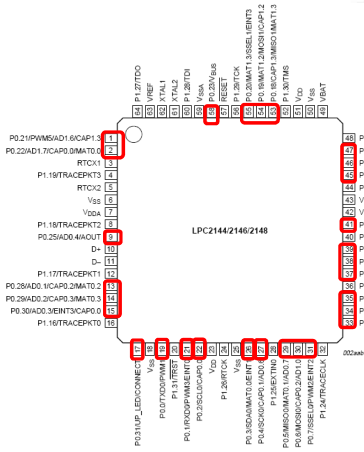
Arquitetura (LPC2368)

- Core do ARM7TDMI-S
- Flash Memory 512kB
- SRAM Memory 58kB
- System Control Block
- Interrupt Controller
- AMBA-AHB Bus
- VPB Peripheral Bus

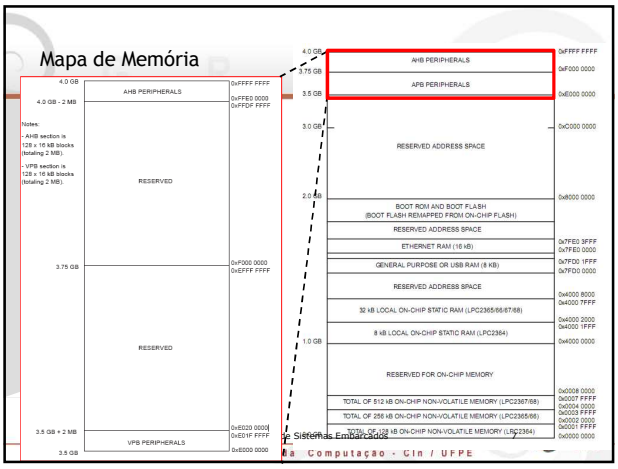


Pinagem

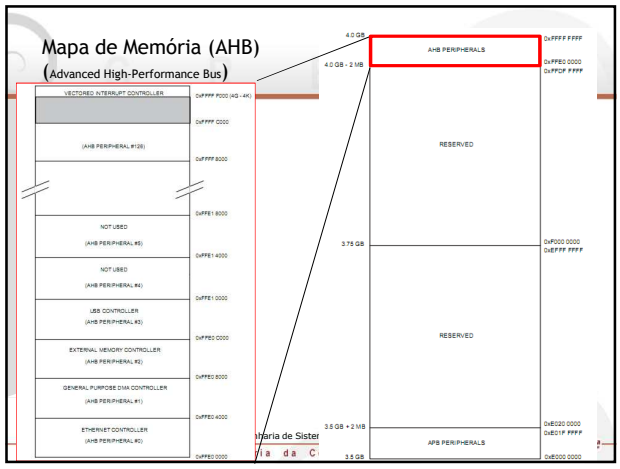
- P0 - 32 I/O pins



Mapa de Memória

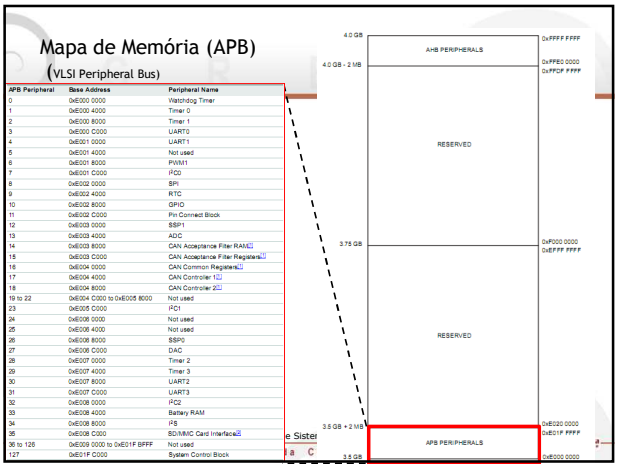


Mapa de Memória (AHB)
(Advanced High-Performance Bus)

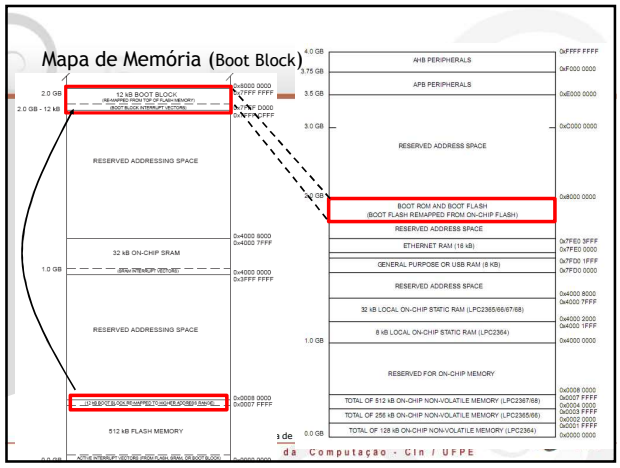


Mapa de Memória (APB)
(VLSI Peripheral Bus)

APB Peripheral	Base Address	Peripheral Name
0	0xE000 0000	Watchdog Timer
1	0xE000 4000	Timer 0
2	0xE000 8000	Timer 1
3	0xE000 C000	UART0
4	0xE001 0000	UART1
5	0xE001 4000	Not used
6	0xE001 8000	PWM1
7	0xE001 C000	I²C0
8	0xE002 0000	SPI
9	0xE002 4000	RTC
10	0xE002 8000	GPIO
11	0xE002 C000	Pin Connect Block
12	0xE003 0000	SSP1
13	0xE003 4000	ADC
14	0xE003 8000	CAN Acceptance Filter RAM[2]
15	0xE003 C000	CAN Acceptance Filter Registers[2]
16	0xE004 0000	CAN Common Registers[2]
17	0xE004 4000	CAN Controller 1[2]
18	0xE004 8000	CAN Controller 2[2]
19 to 22	0xE004 C000 to 0xE005 8000	Not used
23	0xE005 C000	I²C1
24	0xE006 0000	Not used
25	0xE006 4000	Not used
26	0xE006 8000	SSP0
27	0xE006 C000	DAC
28	0xE007 0000	Timer 2
29	0xE007 4000	Timer 3
30	0xE007 8000	UART2
31	0xE007 C000	UART3
32	0xE008 0000	I²C2
33	0xE008 4000	Battery RAM
34	0xE008 8000	I²S
35	0xE008 C000	SD/MMC Card Interface[3]
36 to 126	0xE009 0000 to 0xE01F BFFF	Not used
127	0xE01F C000	System Control Block

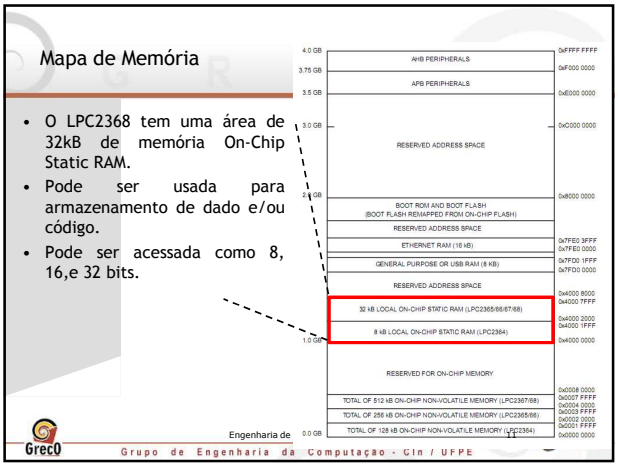


Mapa de Memória (Boot Block)



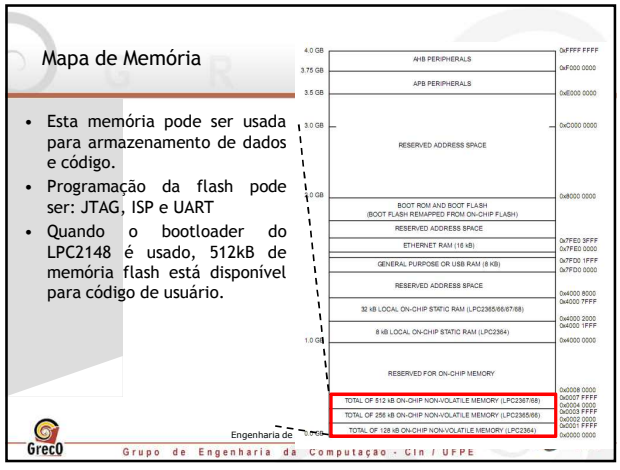
Mapa de Memória

- O LPC2368 tem uma área de 32kB de memória On-Chip Static RAM.
- Pode ser usada para armazenamento de dado e/ou código.
- Pode ser acessada como 8, 16,e 32 bits.



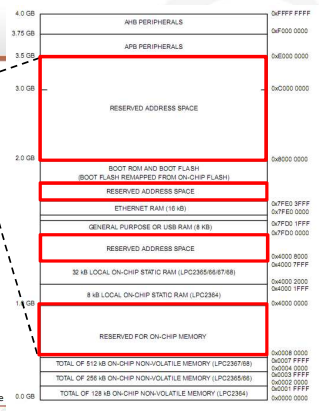
Mapa de Memória

- Esta memória pode ser usada para armazenamento de dados e código.
- Programação da flash pode ser: JTAG, ISP e UART
- Quando o bootloader do LPC2148 é usado, 512kB de memória flash está disponível para código de usuário.



Mapa de Memória

- O LPC2368 gera uma *abort exception* se for feito um acesso para uma região de endereço reservado.



Controle de Mapeamento de Memória

- O controle de mapeamento de memória altera o mapeamento dos vetores de interrupção que aparecem no endereço 0x0000 0000.
- Isto permite executar o código em diferentes espaços de memória.

Mode	Activation	Usage
Boot	Hardware	The Boot Loader always executes after any reset. The Boot ROM m of memory to allow during the Boot Loading he Boot Flash) is available to
		ld User Program Signature is operation is not forced. are found in the bottom of the
		Interrupt vectors are AM.
		Interrupt vectors are
Memory mode	user code	

Bit	Symbol	Value	Description	Reset value
1:0	MAP	00	Boot Loader Mode. Interrupt vectors are re-mapped to Boot ROM.	00
		01	User Flash Mode. Interrupt vectors are not re-mapped and reside in Flash.	
		10	User RAM Mode. Interrupt vectors are re-mapped to Static RAM.	
		11	User External Memory Mode (available on LPC2377/78 and LPC2388 only).	
			Warning: Improper setting of this value may result in incorrect operation of the device.	

Bloco de Controle do Sistema

- System Control Block
  - Bloco para controle de várias funções e registradores:
    - Cristal Oscilador
    - Entrada de Interrupções Externas
    - Controle de Mapeamento de Memória
    - PLL
    - Controle de Potência
    - Reset
    - Divisor VPB
    - Timer Wakeup

Bloco de Controle do Sistema

- Pinos associados ao "System Control Block"

Pin name	Pin direction	Pin description
X1	Input	**Crystal Oscillator Input** - Input to the oscillator and internal clock generator circuits
X2	Output	**Crystal Oscillator Output** - Output from the oscillator amplifier
EINT0	Input	**External Interrupt Input 0** - An active low/high level or falling/rising edge general purpose interrupt input. This pin may be used to wake up the processor from Idle or Power-down modes. Pins P0.1 and P0.16 can be selected to perform EINT0 function.
EINT1	Input	**External Interrupt Input 1** - See the EINT0 description above. Pins P0.3 and P0.14 can be selected to perform EINT1 function. **Important:** LOW level on pin P0.14 immediately after reset is considered as an external hardware request to start the ISP command handler.
EINT2	Input	**External Interrupt Input 2** - See the EINT0 description above. Pins P0.7 and P0.15 can be selected to perform EINT2 function.
EINT3	Input	**External Interrupt Input 3** - See the EINT0 description above. Pins P0.9, P0.20 and P0.30 can be selected to perform EINT3 function.
RESET	Input	**External Reset input** - A LOW on this pin resets the chip, causing I/O ports and peripherals to take on their default states, and the processor to begin execution at address 0x0000 0000.

Obs: Mais de um pino pode ser usado para desempenhar tais interrupções

Crystal Oscillator

- Modos de operação dos osciladores:
  - Cristal externo (Xtal)
  - Alimentando o X1 por um gerador de clock
- Se o sistema PLL ou boot-loader estiver sendo usado, a frequência é limitada de 10 a 25MHz.

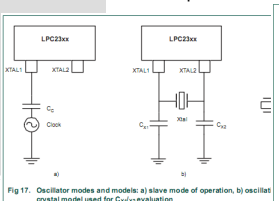


Fig 17. Oscillator modes and models: a) slave mode of operation, b) oscillat crystal model used for $C_{X1/X2}$ evaluation

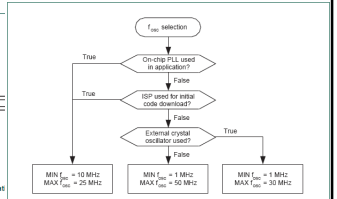


Fig 7. F_{OSC} selection algorithm

Registradores da Interrupção Externa

Table 18. External Interrupt registers

Name	Description
EXTINT	The External Interrupt Flag Register contains interrupt flags for EINT0, EINT1, EINT2 and EINT3. See Table 3–19.
EXTMODE	The External Interrupt Mode Register control whether each pin is edge- or level-sensitive. See Table 3–20.
EXTPOLAR	The External Interrupt Polarity Register contro which level or edge on each pin will cause ar interrupt. See Table 3–21.

Table 19. External Interrupt Flag register (EXTINT - address 0xE01F C140) bit description

Bit	Symbol	Description	Reset value
0	EINT0	In level-sensitive mode, this bit is set if the EINT0 function is selected for its	0

Bit	Symbol	Value	Description	Reset value
0	EXTPOLAR0	0	EINT0 is low-active or falling-edge sensitive (depending on EXTMODE0).	0
		1	EINT0 is high-active or rising-edge sensitive (depending on EXTMODE0).	
1	EXTPOLAR1	0	EINT1 is low-active or falling-edge sensitive (depending on EXTMODE1).	0
		1	EINT1 is high-active or rising-edge sensitive (depending on EXTMODE1).	
2	EXTPOLAR2	0	EINT2 is low-active or falling-edge sensitive (depending on EXTMODE2).	0
		1	EINT2 is high-active or rising-edge sensitive (depending on EXTMODE2).	
3	EXTPOLAR3	0	EINT3 is low-active or falling-edge sensitive (depending on EXTMODE3).	0
			This bit is cleared by writing a one to it, except in level sensitive mode when the pin is in its active state.[1]	
7:4	-		Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA

Se é ativo em

Clock and Power Control

- Oscillators
- Clock Source Selection
- PLL
- Clock Dividers
- Power Control
- Wakeup Timer

Table 32. Summary of system control registers

Name	Description	Access	Reset value	Address
Clock source selection				
CLKSRCSEL	Clock Source Select Register	R/W	0	0xE01F C10C
Phase Locked Loop				
PLLCON	PLL Control Register	R/W	0	0xE01F C080
PLLCFG	PLL Configuration Register	R/W	0	0xE01F C084
PLLSTAT	PLL Status Register	RO	0	0xE01F C088
PLLFEED	PLL Feed Register	WO	NA	0xE01F C08C
Clock dividers				
CCLKCFG	CPU Clock Configuration Register	R/W	0	0xE01F C104
USBCLKCFG	USB Clock Configuration Register	R/W	0	0xE01F C108
IRCTRIM	IRC Trim Register	R/W	0xA0	0xE01FC1A4
PCLKSEL0	Peripheral Clock Selection register 0.	R/W	0	0xE01F C1A8
PCLKSEL1	Peripheral Clock Selection register 1.	R/W	0	0xE01F C1AC
Power control				
PCON	Power Control Register	R/W	0	0xE01F C0C0
INTWAKE	Interrupt Wakeup Register	R/W	0	0xE01F C144
PCONP	Power Control for Peripherals Register	R/W	0x03BE	0xE01F C0C4

Clock Source Select Register

- As fontes de clock disponíveis são:
  - oscilador principal
    - Usado como fonte da CPU com ou sem uso de PLL
    - Opera de 1 a 24MHz (pode ser aumentanda)
  - oscilador RTC
    - Usado para o watchdog timer ou clock para CPU
  - oscilador RC interno.
    - Usado para o watchdog timer ou clock para CPU
    - A precisão dele não permite que seja usado para USB
    - Também não dá para ser usado para CAN se for necessário baud rate ma
    - Frequência n

Table 35. Clock Source Select register (CLKSRCSEL - address 0xE01F C10C) bit description

Bit	Symbol	Value	Description	Reset value
1:0	CLKSRC		Selects the clock source for the PLL as follows:	0
		00	Selects the internal RC oscillator as the PLL clock source (default).	
		01	Selects the main oscillator as the PLL clock source.	
		10	Selects the RTC oscillator as the PLL clock source.	
		11	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	
			Warning: Improper setting of this value, or an incorrect sequence of changing this value may result in incorrect operation of the device.	
7:2	-		Unused, always 0.	0

PLL (Phase Locked Loop)

- Aceita uma frequência de clock em uma escala que varia de 32kHz até 25MHz.
- A frequência de entrada é multiplicada para uma alta frequência e em seguida dividida para uma baixa para prover clock para USB (48MHz) e CPU (até 72MHz).

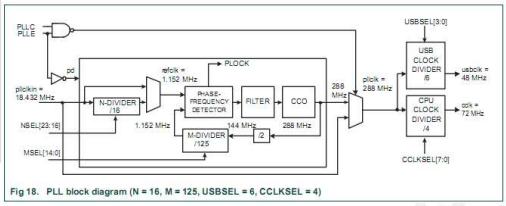


Fig 18. PLL block diagram (N = 16, M = 125, USBSEL = 6, CCLKSEL = 4)

PLL (Phase Locked Loop)

Table 36. PLL registers

Name	Description	Access	Reset value[1]	Address
PLLCFG	PLL Configuration Register. Holding register for updating PLL configuration values. Values written to this register do not take effect until a valid PLL feed sequence has taken place.	R/W	0	0xE01F C084
PLLSTAT	PLL Status Register. Read-back register for PLL control and configuration information. If PLLCON or PLLCFG have been written to, but a PLL feed sequence has not yet occurred, they will not reflect the current PLL state. Reading this register provides the actual values controlling the PLL, as well as the PLL status.	RO	0	0xE01F C088
PLLFEED	PLL Feed Register. This register enables loading of the PLL control and configuration information from the PLLCON and PLLCFG registers into the shadow registers that actually affect PLL operation.	WO	NA	0xE01F C08C
PLLCON	PLL Control Register. Holding register for updating PLL control bits. Values written to this register do not take effect until a valid PLL feed sequence has taken place.	R/W	0	0xE01F C080

- Uma sequência válida (0xAA e 0x55) no registrador PLLFEED precisa acontecer para permitir operações com registradores:
  - PLLCON = para habilitar e conectar PLL
  - PLLCFG = para configurar (multiplic. e divisão do PLL)
- Modos PLL e Power-Down
  - O modo power-down desconecta automaticamente os PLLs ativados
  - Do *power-down* para o *wake-up* não restaura as configurações dos PLLs, isso precisa ser feito via sw.

Power Control

- O LPC2148 suporta 3 modos de redução de potência:
  - Idle Mode
  - Sleep Mode
  - Power-down Mode
- No modo Idle, execução de instruções é suspensa até um reset ou interrupção ocorrer. O clock do core de parado.
  - Funções periféricas continuam em operação durante o modo Idle e podem gerar interrupções.
- No modo Sleep, o oscilador principal é desligado e todos os clocks são parados.
  - A saída do IRC é desabilitada mas o IRC não é desligado para rápido wakeup futuro, bem como o clock do RTC
- No modo Power-Down o oscilador é desligado e o chip não recebe sinais internos do clock.
  - O estado do processador e registradores, valores internos da SRAM são preservados.
  - O nível lógico dos pinos do chip permanecem estáticos.
  - A condição de wake-up de uma interrupção externa causa um restart do clock.
  - O power-down também pode ser terminado com reset.

Registradores Power

Table 52. Power Control registers

Name	Description
PCON	Power Control Register. This register contains control bits that enable the m reduced power operating modes of th LPC2300. See Table 4–53.
INTWAKE	Interrupt Wakeup Register. Controls w interrupts will wake the LPC2300 from power-down mode. See Table 4–55
PCONP	Power Control for Peripherals Regist register contains control bits that enab disable individual peripheral functions allowing elimination of power consump peripherals that are not needed.

Table 56. Power Control for Peripherals register (PCONP - address 0xE01F C0C4) bit description

Bit	Symbol	Description	Reset value
0	-	Unused, always 0.	0
1	PCTIM0	Timer/Counter 0 power/clock control bit.	1
2	PCTIM1	Timer/Counter 1 power/clock control bit.	1
3	PCUART0	UART0 power/clock control bit.	1
4	PCUART1	UART1 power/clock control bit.	1
5	-	Unused, always 0.	1
6	PCPWM1	PWM1 power/clock control bit.	1
7	PCI2C0	The I2C0 interface power/clock control bit.	1
8	PCSPI	The SPI interface power/clock control bit.	1
9	PCRTC	The RTC power/clock control bit.	1
10	PCSSP1	The SSP1 interface power/clock control bit.	1
11	PCEMC	External Memory Controller	1
12	PCAD	A/D converter (ADC) power/clock control bit. **Note:** Clear the PDN bit in the AD0CR (see Section 27–6.1) before clearing this bit, and set this bit before setting PDN.	0
13	PCAN1	CAN Controller 1 power/clock control bit.	0
14	PCAN2	CAN Controller 2 power/clock control bit.	0
18:15	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA
19	PCI2C1	The I2C1 interface power/clock control bit.	1
20	-	Unused, always 0	0
21	PCSSP0	The SSP0 interface power/clock control bit.	1
22	PCTIM2	Timer 2 power/clock control bit.	0
23	PCTIM3	Timer 3 power/clock control bit.	0
24	PCUART2	UART 2 power/clock control bit.	0
25	PCUART3	UART 3 power/clock control bit.	0
26	PCI2C2	I2C interface 2 power/clock control bit.	1
27	PCI2S	I2S interface power/clock control bit.	0
28	PCSDC	SD card interface power/clock control bit.	0
29	PCGPDMA	GP DMA function power/clock control bit.	0
30	PCENET	Ethernet block power/clock control bit.	0
31	PCUSB	USB interface power/clock control bit.	0

Pin Connect Block

- O bloco de conexão do pino permite selecionar pinos do microcontrolador para ter mais do que uma função.
- Registradores de configuração controlam os multiplexadores para permitir conexão entre pinos e os periféricos do chip.
- Seleção de uma função na porta do pino exclui todas as outras funções.
- Módulo com 2 registradores:
  - PINSEL0, PINSEL1, PINSEL2, PINSEL3 e PINSEL4

Table 102. Pin function select register bits

PINSEL0 to PINSEL9 Values	Function	Value after Reset
00	Primary (default) function, typically GPIO port	00
01	First alternate function	
10	Second alternate function	
11	Third alternate function	

PINMODE

- Controla características de pull-up e pull-down de todas as portas.

The PINMODE registers control the on-chip pull-up/pull-down resistor feature (the mode) for all ports. The on-chip pull-up/pull-down resistor can be selected for every pin regardless of the function on this pin with the exception of the I^2C pins and the USB pins (see Section 9–5.13). Two bits are used to control the mode of a port pin. Bits are reserved for unused pins as in the PINSEL registers.

Table 103. Pin Mode Select register Bits

PINMODE0 to PINMODE9 Values	Function	Value after Reset
00	Pin has an on-chip pull-up resistor enabled.	00
01	Reserved. This value should not be used.	
10	Pin has neither pull-up nor pull-down resistor enabled.	
11	Pin has an on-chip pull-down resistor enabled.	

Registrador PINSEL0

PINSEL0	Pin name	Function when 00	Function when 01	Function when 10	Function when 11	Reset value
1:0	P0.0	GPIO Port 0.0	RD1[1]	TXD3	SDA1	00
3:2	P0.1	GPIO Port 0.1	TD1[1]	RXD3	SCL1	00
5:4	P0.2	GPIO Port 0.2	TXD0	Reserved	Reserved	00
7:6	P0.3	GPIO Port 0.3	RXD0	Reserved	Reserved	00
9:8	P0.4	GPIO Port 0.4	I2SRX_CLK	RD2[1]	CAP2.0	00
11:10	P0.5	GPIO Port 0.5	I2SRX_WS	TD2[1]	CAP2.1	00
13:12	P0.6	GPIO Port 0.6	I2SRX_SDA	SSEL1	MAT2.0	00
15:14	P0.7	GPIO Port 0.7	I2STX_CLK	SCK1	MAT2.1	00
17:16	P0.8	GPIO Port 0.8	I2STX_WS	MISO1	MAT2.2	00
19:18	P0.9	GPIO Port 0.9	I2STX_SDA	MOSI1	MAT2.3	00
21:20	P0.10	GPIO Port 0.10	TXD2	SDA2	MAT3.0	00
23:22	P0.11	GPIO Port 0.11	RXD2	SCL2	MAT3.1	00
25:24	-	Reserved	Reserved	Reserved	Reserved	00
27:26	-	Reserved	Reserved	Reserved	Reserved	00
29:28	-	Reserved	Reserved	Reserved	Reserved	00
31:30	P0.15	GPIO Port 0.15	TXD1	SCK0	SCK	00

Registrador PINSEL1

Table 107. Pin function select register 1 (PINSEL1 - address 0xE002 C004) bit description (LPC2364/65/66/67/68 and LPC2387)

PINSEL1	Pin name	Function when 00	Function when 01	Function when 10	Function when 11	Reset value
1:0	P0.16	GPIO Port 0.16	RXD1	SSEL0	SSEL	00
3:2	P0.17	GPIO Port 0.17	CTS1	MISO0	MISO	00
5:4	P0.18	GPIO Port 0.18	DCD1	MOSI0	MOSI	00
7:6	P0.19	GPIO Port 0.19	DSR1	MCICLK	SDA1	00
9:8	P0.20	GPIO Port 0.20	DTR1	MCICMD	SCL1	00
11:10	P0.21	GPIO Port 0.21	RI1	MCIPWR	RD1[1]	00
13:12	P0.22	GPIO Port 0.22	RTS1	MCIDAT0	TD1[1]	00
15:14	P0.23	GPIO Port 0.23	AD0.0	I2SRX_CLK	CAP3.0	00
17:16	P0.24	GPIO Port 0.24	AD0.1	I2SRX_WS	CAP3.1	00
19:18	P0.25	GPIO Port 0.25	AD0.2	I2SRX_SDA	TXD3	00
21:20	P0.26	GPIO Port 0.26	AD0.3	AOUT	RXD3	00
23:22	P0.27[3]	GPIO Port 0.27	SDA0	Reserved	Reserved	00
25:24	P0.28[3]	GPIO Port 0.28	SCL0	Reserved	Reserved	00
27:26	P0.29	GPIO Port 0.29	USB_D+1	Reserved	Reserved	00
29:28	P0.30	GPIO Port 0.30	USB_D−1	Reserved	Reserved	00
31:30	P0.31	Reserved	Reserved	Reserved	Reserved	00

Registrador PINSEL2

Table 109. Pin function select register 2 (PINSEL2 - address 0xE002 C008) bit description (LPC2364/65/66/67/68, LPC2377/78, LPC2387, LPC2388)

PINSEL2	Pin name	Function when 00	Function when 01	Function when 10	Function when 11	Reset value
1:0	P1.0	GPIO Port 1.0	ENET_TXD0	Reserved	Reserved	00
3:2	P1.1	GPIO Port 1.1	ENET_TXD1	Reserved	Reserved	00
5:4	P1.2	Reserved	Reserved	Reserved	Reserved	00
7:6	P1.3	Reserved	Reserved	Reserved	Reserved	00
9:8	P1.4	GPIO Port 1.4	ENET_TX_EN	Reserved	Reserved	00
11:10	P1.5	Reserved	Reserved	Reserved	Reserved	00
13:12	P1.6	Reserved	Reserved	Reserved	Reserved	00
15:14	P1.7	Reserved	Reserved	Reserved	Reserved	00
17:16	P1.8	GPIO Port 1.8	ENET_CRS	Reserved	Reserved	00
19:18	P1.9	GPIO Port 1.9	ENET_RXD0	Reserved	Reserved	00
21:20	P1.10	GPIO Port 1.10	ENET_RXD1	Reserved	Reserved	00
23:22	P1.11	Reserved	Reserved	Reserved	Reserved	00
25:24	P1.12	Reserved	Reserved	Reserved	Reserved	00
27:26	P1.13	Reserved	Reserved	Reserved	Reserved	00
29:28	P1.14	GPIO Port 1.14	ENET_RX_ER	Reserved	Reserved	00
31:30	P1.15	GPIO Port 1.15	ENET_REF_CLK	Reserved	Reserved	00

Registrador PINSEL3

Table 110. Pin function select register 3 (PINSEL3 - address 0xE002 C00C) bit description (LPC2361/62/64/65/66/67/68 and LPC2387)

PINSEL3	Pin name	Function when 00	Function when 01	Function when 10	Function when 11	Reset value
1:0	P1.16	GPIO Port 1.16	ENET_MDC	Reserved	Reserved	00
3:2	P1.17	GPIO Port 1.17	ENET_MDIO	Reserved	Reserved	00
5:4	P1.18	GPIO Port 1.18	USB_UP_LED1[2]	PWM1.1	CAP1.0	00
7:6	P1.19	GPIO Port 1.19	USB_TX_E1[2]	USB_PPWR1[2]	CAP1.1	00
9:8	P1.20	GPIO Port 1.20	USB_TX_DP1[2]	PWM1.2	SCK0	00
11:10	P1.21	GPIO Port 1.21	USB_TX_DM1[2]	PWM1.3	SSEL0	00
13:12	P1.22	GPIO Port 1.22	USB_RCV1[2]	USB_PWRD1[3]	MAT1.0	00
15:14	P1.23	GPIO Port 1.23	USB_RX_DP1[2]	PWM1.4	MISO0	00
17:16	P1.24	GPIO Port 1.24	USB_RX_DM1[2]	PWM1.5	MOSI0	00
19:18	P1.25	GPIO Port 1.25	USB_LS1[2]	USB_HSTEN1[3]	MAT1.1	00
21:20	P1.26	GPIO Port 1.26	USB_SSPND1[2]	PWM1.6	CAP0.0	00
23:22	P1.27	GPIO Port 1.27	USB_INT1[2]	USB_OVRCRT1[3]	CAP0.1	00
25:24	P1.28	GPIO Port 1.28	USB_SCL1[2]	PCAP1.0	MAT0.0	00
27:26	P1.29	GPIO Port 1.29	USB_SDA1[2]	PCAP1.1	MAT0.1	00
29:28	P1.30	GPIO Port 1.30	Reserved	V_{BUS}[3]	AD0.4	00
31:30	P1.31	GPIO Port 1.31	Reserved	SCK1	AD0.5	00

Registrador PINSEL4

Table 112. Pin function select register 4 (PINSEL4 - address 0xE002 C010) bit description (LPC2364/65/66/67/68 and LPC2387)

PINSEL4	Pin name	Function when 00	Function when 01	Function when 10	Function when 11	Reset value
1:0	P2.0	GPIO Port 2.0	PWM1.1	TXD1	TRACECLK[1]	00
3:2	P2.1	GPIO Port 2.1	PWM1.2	RXD1	PIPESTAT0[1]	00
5:4	P2.2	GPIO Port 2.2	PWM1.3	CTS1	PIPESTAT1[1]	00
7:6	P2.3	GPIO Port 2.3	PWM1.4	DCD1	PIPESTAT2[1]	00
9:8	P2.4	GPIO Port 2.4	PWM1.5	DSR1	TRACESYNC[1]	00
11:10	P2.5	GPIO Port 2.5	PWM1.6	DTR1	TRACEPKT0[1]	00
13:12	P2.6	GPIO Port 2.6	PCAP1.0	RI1	TRACEPKT1[1]	00
15:14	P2.7	GPIO Port 2.7	RD2[2]	RTS1	TRACEPKT2[1]	00
17:16	P2.8	GPIO Port 2.8	TD2[2]	TXD2	TRACEPKT3[1]	00
19:18	P2.9	GPIO Port 2.9	USB_CONNECT1[2]	RXD2	EXTIN0[1]	00
21:20	P2.10	GPIO Port 2.10	EINT0	Reserved	Reserved	00
23:22	P2.11	GPIO Port 2.11	EINT1	MCIDAT1	I2STX_CLK	00
25:24	P2.12	GPIO Port 2.12	EINT2	MCIDAT2	I2STX_WS	00
27:26	P2.13	GPIO Port 2.13	EINT3	MCIDAT3	I2STX_SDA	00
29:28	P2.14	Reserved	Reserved	Reserved	Reserved	00
31:30	P2.15	Reserved	Reserved	Reserved	Reserved	00

GPIO (General Purpose Input/Output Ports)

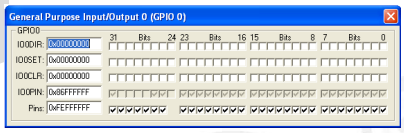
- Portas programáveis de entrada e saída de dados.
- Entradas e saídas de propósito geral
- Usadas para prover uma interface entre os periféricos e os microcontroladores.
- O número de GPIOs disponíveis depende do uso de funções alternativas.

Table 131. GPIO pin description

Pin Name	Type	Description
P0[31:0] P1[31:0] P2[31:0] P3[31:0] P4[31:0]	Input/ Output	General purpose input/output. These are typically shared with other peripherals functions and will therefore not all be available in an application. Packaging options may affect the number of GPIOs available in a particular device (see Table 1–2 and Table 9–101). Some pins may be limited by requirements of the alternate functions of the pin. For example, the pins containing the I^2C0 function are open-drain for any function of that pin. Details may be found in the LPC2300 pin description.

GPIO (General Purpose Input/Output Ports)

- Registradores:
  - IO0DIR: Registrador que associa a direção de cada bit I/O do Port. Se "1" configurado como saída e se "0" configurado como entrada.
  - IO0SET: Setar com "1", força nível alto para aquele bit da porta durante a saída.
  - IO0CLR: Setar com "1", força nível baixo para aquele bit da porta durante a saída
  - IOPIN: Contém o valor atual dos pinos

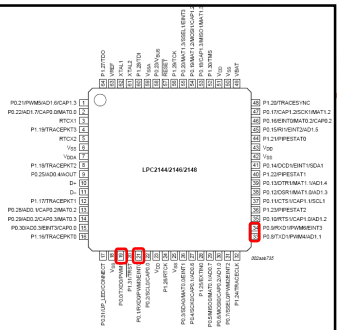


CAN (Controller Area Network)

- Protocolo de comunicação High Performance para comunicação de dados serial.
- Suporta controle em tempo real distribuído com alto nível de segurança.
- Usados em ambientes industriais, automotivos e redes de alta velocidade.

UART

- Pino 19: TXD0 - UART0
- Pino 21: RXD0 - UART0
- Pino 33: TXD1 - UART1
- Pino 34: RXD1 - UART1



UART0

Bit	Symbol	Description	Reset value
7:0	RBR	The UART0 Receiver Buffer Register contains the oldest received byte in the UART0 Rx FIFO.	undefined

Name	Description	Bit functions and addresses MSB BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	LSB BIT0	Access	Reset value[1]	Address
U0RBR	Receiver Buffer Register	8-bit Read Data								RO	NA	0xE000 C000 (DLAB=0)
U0THR	Transmit Holding Register	8-bit Write Data								WO	NA	0xE000 C000 (DLAB=0)
U0DLL	Divisor Latch LSB	8-bit Data								R/W	0x01	0xE000 C000 (DLAB=1)
U0DLM	Divisor Latch MSB	8-bit Data								R/W	0x00	0xE000 C004 (DLAB=1)
U0IER	Interrupt Enable Register	-	-	-	-	-	-	En.ABTO Int	En.ABEO Int	R/W	0x00	0xE000 C004 (DLAB=0)
		-	-	-	-	-	En.RX Lin.St.Int	Enable THRE Int	En.RX Dat.Av.Int			
U0IIR	Interrupt ID Reg.	-	-	-	-	-	-	ABTO Int	ABEO Int	RO	0x01	0xE000 C008
		FIFOs Enabled		-	-	IIR3	IIR2	IIR1	IIR0			
U0FCR	FIFO Control Register	RX Trigger		-	-	-	TX FIFO Reset	RX FIFO Reset	FIFO Enable	WO	0x00	0xE000 C008
U0LCR	Line Control Register	DLAB	Set Break	Stick Parity	Even Par.Selct.	Parity Enable	No. of Stop Bits	Word Length Select		R/W	0x00	0xE000 C00C
U0LSR	Line Status Register	RX FIFO Error	TEMT	THRE	BI	FE	PE	OE	DR	RO	0x60	0xE000 C014
U0SCR	Scratch Pad Reg.	8-bit Data								R/W	0x00	0xE000 C01C
U0ACR	Auto-baud Control Register	-	-	-	-	-	-	ABTO Int.Clr	ABEO Int.Clr	R/W	0x00	0xE000 C020
		-	-	-	-	-	Aut.Rstrt.	Mode	Start			
U0FDR	Fractional Divider Register	Reserved[31:8]									0x10	0xE000 C028
		MulVal				DivAddVal						
U0TER	TX. Enable Reg.	TXEN	-	-	-	-	-	-	-	R/W	0x80	0xE000 C030

UART0

Bit	Symbol	Description	Reset value
7:0	THR	Writing to the UART0 Transmit Holding Register causes the data to be stored in the UART0 transmit FIFO. The byte will be sent when it reaches the bottom of the FIFO and the transmitter is available.	NA

Name	Description	Bit functions and addresses MSB BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	LSB BIT0	Access	Reset value[1]	Address
U0RBR	Receiver Buffer Register	8-bit Read Data								RO	NA	0xE000 C000 (DLAB=0)
U0THR	Transmit Holding Register	8-bit Write Data								WO	NA	0xE000 C000 (DLAB=0)
U0DLL	Divisor Latch LSB	8-bit Data								R/W	0x01	0xE000 C000 (DLAB=1)
U0DLM	Divisor Latch MSB	8-bit Data								R/W	0x00	0xE000 C004 (DLAB=1)
U0IER	Interrupt Enable Register	-	-	-	-	-	-	En.ABTO Int	En.ABEO Int	R/W	0x00	0xE000 C004 (DLAB=0)
		-	-	-	-	-	En.RX Lin.St.Int	Enable THRE Int	En.RX Dat.Av.Int			
U0IIR	Interrupt ID Reg.	-	-	-	-	-	-	ABTO Int	ABEO Int	RO	0x01	0xE000 C008
		FIFOs Enabled		-	-	IIR3	IIR2	IIR1	IIR0			
U0FCR	FIFO Control Register	RX Trigger		-	-	-	TX FIFO Reset	RX FIFO Reset	FIFO Enable	WO	0x00	0xE000 C008
U0LCR	Line Control Register	DLAB	Set Break	Stick Parity	Even Par.Selct.	Parity Enable	No. of Stop Bits	Word Length Select		R/W	0x00	0xE000 C00C
U0LSR	Line Status Register	RX.FIFO Error	TEMT	THRE	BI	FE	PE	OE	DR	RO	0x60	0xE000 C014
U0SCR	Scratch Pad Reg.	8-bit Data								R/W	0x00	0xE000 C01C
U0ACR	Auto-baud Control Register	-	-	-	-	-	-	ABTO Int.Clr	ABEO Int.Clr	R/W	0x00	0xE000 C020
		-	-	-	-	-	Aut.Rstrt.	Mode	Start			
U0FDR	Fractional Divider Register	Reserved[31:8]									0x10	0xE000 C028
		MulVal				DivAddVal						
U0TER	TX. Enable Reg.	TXEN	-	-	-	-	-	-	-	R/W	0x80	0xE000 C030

UART0

Bit	Symbol	Description	Reset value
7:0	DLL	The UART0 Divisor Latch LSB Register, along with the U0DLM register, determines the baud rate of the UART0.	0x01

Name	Description	Bit functions and addresses MSB BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	LSB BIT0	Access	Reset value[1]	Address
U0RBR	Receiver Buffer Register	8-bit Read Data								RO	NA	0xE000 C000 (DLAB=0)
U0THR	Transmit Holding Register	8-bit Write Data								WO	NA	0xE000 C000 (DLAB=0)
U0DLL	Divisor Latch LSB	8-bit Data								R/W	0x01	0xE000 C000 (DLAB=1)
U0DLM	Divisor Latch MSB	8-bit Data								R/W	0x00	0xE000 C004 (DLAB=1)
U0IER	Interrupt Enable Register	-	-	-	-	-	-	En.ABTO Int	En.ABEO Int	R/W	0x00	0xE000 C004 (DLAB=0)
		-	-	-	-	-	En.RX Lin.St.Int	Enable THRE Int	En.RX Dat.Av.Int			
U0IIR	Interrupt ID Reg.	-	-	-	-	-	-	ABTO Int	ABEO Int	RO	0x01	0xE000 C008
		FIFOs Enabled		-	-	IIR3	IIR2	IIR1	IIR0			
U0FCR	FIFO Control Register	RX Trigger		-	-	-	TX FIFO Reset	RX FIFO Reset	FIFO Enable	WO	0x00	0xE000 C008
U0LCR	Line Control Register	DLAB	Set Break	Stick Parity	Even Par.Selct.	Parity Enable	No. of Stop Bits	Word Length Select		R/W	0x00	0xE000 C00C
U0LSR	Line Status Register	RX.FIFO Error	TEMT	THRE	BI	FE	PE	OE	DR	RO	0x60	0xE000 C014
U0SCR	Scratch Pad Reg.	8-bit Data								R/W	0x00	0xE000 C01C
U0ACR	Auto-baud Control Register	-	-	-	-	-	-	ABTO Int.Clr	ABEO Int.Clr	R/W	0x00	0xE000 C020
		-	-	-	-	-	Aut.Rstrt.	Mode	Start			
U0FDR	Fractional Divider Register	Reserved[31:8]									0x10	0xE000 C028
		MulVal				DivAddVal						
U0TER	TX. Enable Reg.	TXEN	-	-	-	-	-	-	-	R/W	0x80	0xE000 C030

UART0

Bit	Symbol	Description	Reset value
7:0	DLM	The UART0 Divisor Latch MSB Register, along with the U0DLL register, determines the baud rate of the UART0.	0x00

Name	Description	Bit functions and addresses MSB BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	LSB BIT0	Access	Reset value[1]	Address
U0RBR	Receiver Buffer Register	8-bit Read Data								RO	NA	0xE000 C000 (DLAB=0)
U0THR	Transmit Holding Register	8-bit Write Data								WO	NA	0xE000 C000 (DLAB=0)
U0DLL	Divisor Latch LSB	8-bit Data								R/W	0x01	0xE000 C000 (DLAB=1)
U0DLM	Divisor Latch MSB	8-bit Data								R/W	0x00	0xE000 C004 (DLAB=1)
U0IER	Interrupt Enable Register	-	-	-	-	-	-	En.ABTO Int	En.ABEO Int	R/W	0x00	0xE000 C004 (DLAB=0)
		-	-	-	-	-	En.RX Lin.St.Int	Enable THRE Int	En.RX Dat.Av.Int			
U0IIR	Interrupt ID Reg.	-	-	-	-	-	-	ABTO Int	ABEO Int	RO	0x01	0xE000 C008
		FIFOs Enabled		-	-	IIR3	IIR2	IIR1	IIR0			
U0FCR	FIFO Control Register	RX Trigger		-	-	-	TX FIFO Reset	RX FIFO Reset	FIFO Enable	WO	0x00	0xE000 C008
U0LCR	Line Control Register	DLAB	Set Break	Stick Parity	Even Par.Selct.	Parity Enable	No. of Stop Bits	Word Length Select		R/W	0x00	0xE000 C00C
U0LSR	Line Status Register	RX.FIFO Error	TEMT	THRE	BI	FE	PE	OE	DR	RO	0x60	0xE000 C014
U0SCR	Scratch Pad Reg.	8-bit Data								R/W	0x00	0xE000 C01C
U0ACR	Auto-baud Control Register	-	-	-	-	-	-	ABTO Int.Clr	ABEO Int.Clr	R/W	0x00	0xE000 C020
		-	-	-	-	-	Aut.Rstrt.	Mode	Start			
U0FDR	Fractional Divider Register	Reserved[31:8]									0x10	0xE000 C028
		MulVal				DivAddVal						
U0TER	TX. Enable Reg.	TXEN	-	-	-	-	-	-	-	R/W	0x80	0xE000 C030

UART0

Bit	Function	Description	Reset value
3:0	DIVADDVAL	Baudrate generation pre-scaler divisor value. If this field is 0, fractional baudrate generator will not impact the UART0 baudrate.	0
7:4	MULVAL	Baudrate pre-scaler multiplier value. This field must be greater or equal 1 for UART0 to operate properly, regardless of whether the fractional baudrate generator is used or not.	1
31:8	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA

0 < MULVAL ≤ 15
0 ≤ DIVADDVAL ≤ 15

Name	Description	Bit functions a MSB BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	LSB BIT0	s
U0RBR	Receiver Buffer Register	8-bit Read Data								
U0THR	Transmit Holding Register	8-bit Write Data								
U0DLL	Divisor Latch LSB	8-bit Data								
U0DLM	Divisor Latch MSB	8-bit Data								
U0IER	Interrupt Enable Register	-	-	-	-	-	-	En.ABTO Int	En.ABEO Int	
		-	-	-	-	-	En.RX Lin.St.Int	Enable THRE Int	En.RX Dat.Av.Int	
U0IIR	Interrupt ID Reg.	-	-	-	-	-	-	ABTO Int	ABEO Int	
		FIFOs Enabled		-	-	IIR3	IIR2	IIR1	IIR0	
U0FCR	FIFO Control Register	RX Trigger		-	-	-	TX FIFO Reset	RX FIFO Reset	FIFO Enable	
U0LCR	Line Control Register	DLAB	Set Break	Stick Parity	Even Par.Selct.	Parity Enable	No. of Stop Bits	Word Length Select		
U0LSR	Line Status Register	RX.FIFO Error	TEMT	THRE	BI	FE	PE	OE	DR	
U0SCR	Scratch Pad Reg.	8-bit Data								
U0ACR	Auto-baud Control Register	-	-	-	-	-	-	ABTO Int.Clr	ABEO Int.Clr	
		-	-	-	-	-	Aut.Rstrt.	Mode	Start	
U0FDR	Fractional Divider Register	Reserved[31:8]								
		MulVal				DivAddVal				
U0TER	TX. Enable Reg.	TXEN	-	-	-	-	-	-	-	

UART0

Exemplo: baud = 9600

U0DLM = 0x00;
U0DLL = 0x82;

$$UART0_{baudrate} = \frac{PCLK}{16 \times (16 \times U0DLM + U0DLL) \times \left(1 + \frac{DivAddVal}{MulVal}\right)}$$

Table 102: Baudrates available when using 20 MHz peripheral clock (PCLK = 20 MHz)

Desired baudrate	MULVAL = 0 DIVADDVAL = 0 U0DLM:U0DLL hex[2]	dec[1]	% error[3]	Optimal MULVAL & DIVADDVAL U0DLM:U0DLL dec[1]	Fractional pre-scaler value MULDIV / MULDIV + DIVADDVAL	% error[3]
50	61A8	25000	0.0000	25000	1/(1+0)	0.0000
75	411B	16667	0.0020	12500	3/(3+1)	0.0000
110	2C64	11364	0.0032	6250	11/(11+9)	0.0000
134.5	244E	9254	0.0034	3983	3/(3+4)	0.0001
150	208D	8333	0.0040	6250	3/(3+1)	0.0000
300	1047	4167	0.0080	3125	3/(3+1)	0.0000
600	0823	2083	0.0160	1250	3/(3+2)	0.0000
1200	0412	1042	0.0320	625	3/(3+2)	0.0000
1800	02B6	694	0.0640	625	9/(9+1)	0.0000
2000	0271	625	0.0000	625	1/(1+0)	0.0000
2400	0209	521	0.0320	250	12/(12+13)	0.0000
3600	015B	347	0.0640	248	5/(5+2)	0.0064
4800	0104	260	0.1600	125	12/(12+13)	0.0000

Table 102: Baudrates available when using 20 MHz peripheral clock (PCLK = 20 MHz)

Desired baudrate	MULVAL = 0 DIVADDVAL = 0 U0DLM:U0DLL hex[2]	dec[1]	% error[3]	Optimal MULVAL & DIVADDVAL U0DLM:U0DLL dec[1]	Fractional pre-scaler value MULDIV / MULDIV + DIVADDVAL	% error[3]
7200	00AE	174	0.2240	124	5/(5+2)	0.0064
9600	0082	130	0.1600	93	5/(5+2)	0.0064
19200	0041	65	0.1600	31	10/(10+11)	0.0064
38400	0021	33	1.3760	12	7/(7+12)	0.0594
56000	0021	22	1.4400	13	7/(7+5)	0.0160
57600	0016	22	1.3760	19	7/(7+1)	0.0594
112000	000B	11	1.4400	6	7/(7+6)	0.1600
115200	000B	11	1.3760	4	7/(7+12)	0.0594
224000	0006	6	7.5200	3	7/(7+6)	0.1600
448000	0003	3	7.5200	2	5/(5+2)	0.3520

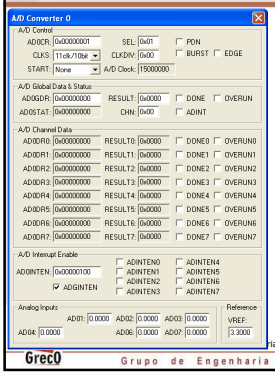
UART0

- Registrador U0LCR
  - Determina o formato do caractere que esta sendo recebido ou enviado.

Table 107: UART0 Line Control Register (U0LCR - address 0xE000 C00C) bit description

Bit	Symbol	Value	Description	Reset value
1:0	Word Length Select	00	5 bit character length	0
		01	6 bit character length	
		10	7 bit character length	
		11	8 bit character length	
2	Stop Bit Select	0	1 stop bit.	0
		1	2 stop bits (1.5 if U0LCR[1:0]=00).	
3	Parity Enable	0	Disable parity generation and checking.	0
		1	Enable parity generation and checking.	
5:4	Parity Select	00	Odd parity. Number of 1s in the transmitted character and the attached parity bit will be odd.	0
		01	Even Parity. Number of 1s in the transmitted character and the attached parity bit will be even.	
		10	Forced "1" stick parity.	
		11	Forced "0" stick parity.	
6	Break Control	0	Disable break transmission.	0
		1	Enable break transmission. Output pin UART0 TXD is forced to logic 0 when U0LCR[6] is active high.	
7	Divisor Latch Access Bit (DLAB)	0	Disable access to Divisor Latches.	0
		1	Enable access to Divisor Latches.	

ARM LPC2148 (Conversor AD)



- Permite especificar a tensão para cada entrada analógica
- Contém os seguintes bits para o controlador AD
  - CLKS: seleciona o número de clocks usados para cada conversão em modo bursrt
  - START: controla quando e se uma conversão AD é iniciada.
  - SEL: seleciona qual pino da entrada analógica será convertida.
  - CLKDIV: Divisor de clock para produzir a taxa AD.
  - PND: power down
  - BURST:

Outros

- TIMER
- USB
- SSP Controller (Synchronous Serial Port)
- SPI Interface (Serial Peripheral Interface)
- I2C Bus
- PWM (Pulse Width Modulator)
- ADC (Analog-to-Digital Converter)
- DAC (Digital-to-Analog Converter)
- Real Time Clock
- Watchdog Timer
- Flash Memory System and Programming

MCB2300