u-blox AG
Zürcherstrasse 68
8800 Thalwil
Switzerland
www.u-blox.com

Phone +41 44 722 7444
Fax +41 44 722 7447
info@u-blox.com

LEA-5
u-blox 5 GPS and GALILEO Modules
Hardware Integration Manual
(incl. Reference Design)

Abstract

This document describes the hardware features and specifications of the u-blox 5 based LEA-5 series of cost effective, high-performance GPS/GALILEO modules.

Features include AssistNow Online and AssistNow Offline A-GPS services, KickStart accelerated acquisition, SuperSense® Indoor GPS providing best-in-class acquisition and tracking sensitivity, precision timing and an innovative jamming-resistant RF architecture. The compact 17.0 x 22.4 mm form factor of the highly successful LEA-4 series is maintained, enabling easy migration. The LEA-5 series supports passive and active antennas.

your position is our focus

Manual

Title	LEA-5	
Subtitle	Hardware Integration Manual	(incl. Reference Design)
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Initial Release	23/04/2008	TG	Addition of Hardware Description, Product Handling, Product Testing, Appendix
A	19/03/2008	TG	Addition of Reference Design. Update to include Eco Power Mode
A1	23/04/2008	TG	USB update

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	Products marked with this lead-free symbol on the product label comply with the "Directive 2002/95/EC of the European Parliament and the Council on the Restriction of Use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS).
	This is an Electrostatic Sensitive Device (ESD). Observe precautions for handling.

Preface

u-blox Technical Documentation

As part of our commitment to customer support, u-blox maintains an extensive volume of technical documentation for our products. In addition to our product-specific technical data sheets, the following manuals are available to assist u-blox customers in product design and development.

- **GPS Compendium:** This document, also known as the GPS book, provides a wealth of information regarding generic GPS questions about system functions and technology.
- **Protocol Specification:** Messages, configuration and functionalities of the u-blox 5 software releases are explained in this document.
- **Hardware Integration Manual:** This Manual provides hardware design instructions and information on how to set up production and final product tests.

How to use this Manual

The LEA-5 Hardware Integration Manual provides the necessary information to successfully design in and configure these u-blox 5-based GPS/GALILEO receiver modules. For navigating this document please note the following:

This manual has a modular structure. It is not necessary to read it from the beginning to the end. To help in finding needed information, a brief section overview is provided below:

1. **Hardware Basics**: This chapter introduces the basics of function and architecture of the LEA 5 modules.
2. **Design-In**: This chapter provides the Design-In information necessary for a successful design.
3. **Product Handling**: This chapter defines packaging, handling, shipment, storage and soldering.
4. **Product Testing**: This chapter provides information about testing of OEM receivers in production.
5. **Appendix:** The Appendix includes a Reference Design, guidelines on how to successfully migrate to u-blox 5 designs, and useful information about the different antenna types available on the market and how to reduce interference in your GPS design.

The following symbols are used to highlight important information within the manual:

☞ An index finger points out key information pertaining to module integration and performance.

⚠ **A warning symbol indicates actions that could negatively impact or damage the module.**

Questions

If you have any questions about u-blox 5 Hardware Integration, please:

- Read this manual carefully.
- Contact our information service on the homepage http://www.u-blox.com
- Read the questions and answers on our FAQ database on the homepage http://www.u-blox.com

Technical Support

Worldwide Web

Our website (www.u-blox.com) is a rich pool of information. Product information, technical documents and helpful FAQ can be accessed 24h a day.

By E-mail

If you have technical problems or cannot find the required information in the provided documents, contact the nearest of the Technical Support offices by email. Use our service pool email addresses rather than any personal email address of our staff. This makes sure that your request is processed as soon as possible. You will find the contact details at the end of the document.

By Phone

If an email contact is not the right choice to solve your problem or does not clearly answer your questions, call the nearest Technical Support office for assistance. You will find the contact details at the end of the document.

Helpful Information when Contacting Technical Support

When contacting Technical Support please have the following information ready:

- Receiver type (e.g. LEA-5A) and firmware version (e.g. V4.00)
- Receiver configuration
- Clear description of your question or the problem together with a u-center logfile
- A short description of the application
- Your complete contact details

Contents

1 Hardware Description

1.1 Functional Overview

The LEA-5 module series is a family of self-contained GPS and GALILEO receivers featuring the powerful 50-channel u-blox 5 positioning engine. These modules provide exceptional GPS performance in a compact form factor and at an economical price. u-blox 5 sets a new standard in GPS receiver technology. A 32-channel acquisition engine with over 1 million effective correlators is capable of massive parallel searches across the time/frequency space. This enables a Time To First Fix (TTFF) of less than 1 second, while long correlation/dwell times make possible the best-in-class acquisition and tracking sensitivity. Once acquired, satellites are passed on to a dedicated tracking engine. This arrangement allows the GPS engine to simultaneously track up to 16 satellites while searching for new ones. u-blox 5's advanced jamming suppression mechanism and innovative RF architecture provide a high level of immunity to jamming, ensuring maximum GPS performance. u-blox 5 has been designed to be able to support the GALILEO system currently being developed by European authorities. The capability of receiving GALILEO L1 signals will provide increased coverage and even better positioning accuracy when this system comes into operation.

With the LEA-5 series the complete signal processing chain from antenna input to serial output is contained within a single component. LEA-5 modules maintain the compact 17.0 x 22.4 mm form factor of their highly successful LEA-4 predecessors. The LEA-5 modules have been designed with backwards compatibility in mind, enabling ease of upgrade and reducing engineering and design costs.

Their small size makes LEA-5 modules the ideal GPS solution for applications with stringent space requirements. The packaging makes expensive RF cabling obsolete, with the RF input being available directly on a pin. The LEA-5 series are SMT solderable and can be handled by standard pick and place equipment.

LEA-5 modules come equipped with a serial port, which can handle NMEA and UBX proprietary data formats, as well as a high speed USB port. The optional FLASH EPROM provides the capacity to store user-specific configuration settings as well as future software updates.

All LEA-5 modules are RoHS compliant (lead-free).

The LEA-5 series of GPS/GALILEO receiver modules are not designed for life saving or supporting devices or for aviation and should not be used in products that could in any way negatively impact the security or health of the user or third parties or that could cause damage to goods.

1.2 Module Selector

u-blox provides several modules using the popular and industry standard LEA Form factor. To select the right product for your design consider Table 1:

	Voltage Range (V)	Thickness (mm)	50-channel engine	KickStart	SuperSense	FW Update / FLASH	Low Power Modes	UART	USB	SPI	DDC	AssistNow Online	AssistNow Offline	Dead Reckoning	Raw Data	Precision Timing	1PPS	CFG Pins	Reset Input	Antenna Supply	Antenna Supervisor
LEA-5H	**2.7-3.6**	**3.0**	✓	✓	✓	✓	**P**	**1**	**1**		**1**	✓	✓				✓		✓	✓	✓
LEA-5S	**2.7-3.6**	**3.0**	✓	✓	✓		**P**	**1**	**P**		**1**	✓	✓				✓	**1**	✓	✓	✓
LEA-5A	**2.7-3.6**	**3.0**	✓		✓		**P**	**1**	**P**		**1**	✓	✓				✓	**1**	✓	✓	✓
LEA-5Q	**2.7-3.6**	**2.4**	✓	✓	✓		**P**	**1**	**1**	**1**	**1**	✓	✓				✓	**3**	✓		
LEA-5M	**2.7-3.6**	**2.4**	✓		✓		**P**	**1**	**1**		**1**	✓	✓				✓	**2**	✓		
LEA-5T	**2.7-3.6**	**3.0**	✓	✓	✓	✓		**1**	**1**		**1**	✓	✓			✓	✓		✓	✓	✓

P= Planned availability Q1/09

Table 1: Features of the LEA-5 Series

1.3 Architecture

LEA-5 modules are divided into two distinct, separately shielded sections. The smaller section is the RF- Section, the larger section contains the Baseband. See Figure 1 for a block diagram of the LEA-5 series.

The RF Front-End contains the integrated Low Noise Amplifier (LNA), the SAW bandpass filter, the u-blox 5 RF-IC and the TCXO or XTO crystal.

The Baseband section contains the digital circuitry comprised of the u-blox 5 Baseband processor, the RTC crystal and additional elements such as the optional FLASH EPROM for enhanced programmability and flexibility.

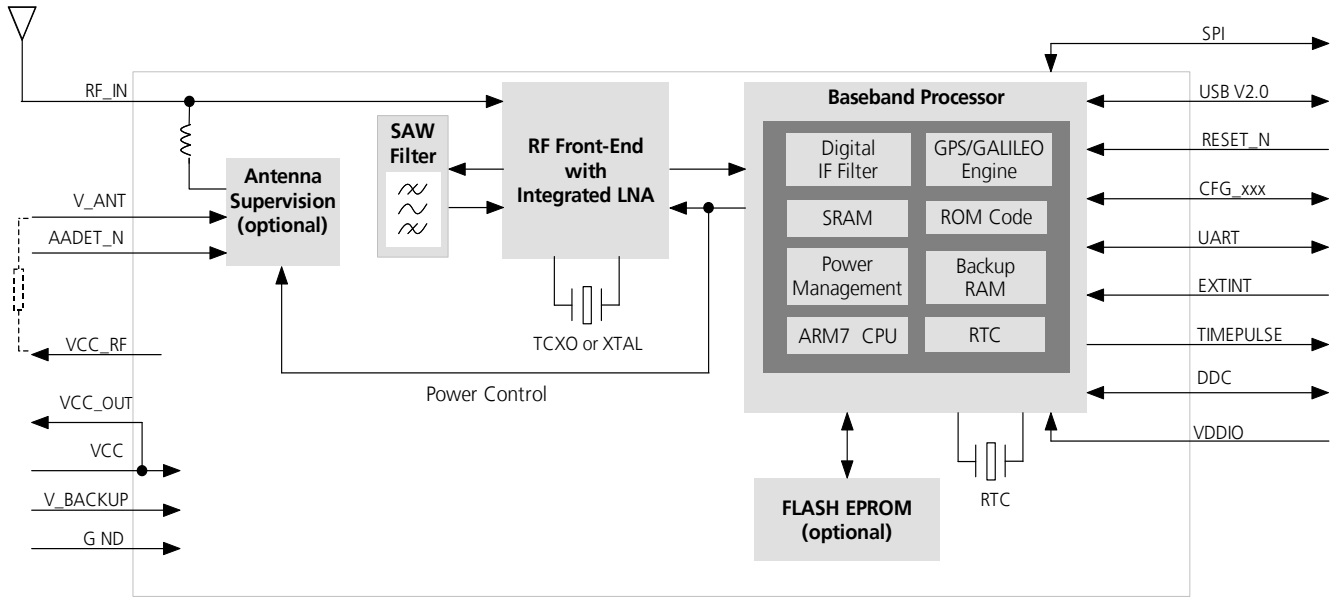


Figure 1: LEA-5 Block Diagram

2 Design-In

☞ For migrating existing ANTARIS®4 product designs to u-blox 5 please refer to *Appendix A*.

In order to obtain good performance with a GPS receiver module, there are a number of points that require careful attention during the design-in. These include:

- Power Supply
  Good performance requires a clean and stable power supply.
- Interfaces
  Ensure correct wiring, rate and message setup on the module and your host system.
- Antenna interface
  For optimal performance seek short routing, matched impedance and no stubs.

2.1 Power Management

2.1.1 Connecting Power

u-blox 5 receivers have three power supply pins: **VCC**, **V_BCKP** and **VDDUSB**.

2.1.1.1 VCC - Main Power

The main power supply is fed through the **VCC** pin. During operation, the current drawn by the u-blox 5 GPS module can vary by some orders of magnitude, especially, if low-power operation modes are enabled. It is important that the system power supply circuitry is able to support the peak power (see datasheet for specification) for a short time. In order to define a battery capacity for specific applications the sustained power figure shall be used.

2.1.1.2 V_BCKP - Backup Battery

In case of a power failure on pin **VCC**, the real-time clock and backup RAM are supplied through pin **V_BCKP**. This enables the u-blox 5 receiver to recover from a power failure with either a Hotstart or a Warmstart (depending on the duration of **VCC** outage) and to maintain the configuration settings. If no backup battery is connected, the receiver performs a Coldstart at power up.

☞ If no backup battery available connect the **V_BCKP** pin to **GND (or VCC)**.

As long as **VCC** is supplied to the u-blox 5 receiver, the backup battery is disconnected from the RTC and the backup RAM in order to avoid unnecessary battery drain (see Figure 2). Power to RTC and BBR is supplied from **VCC** in this case.

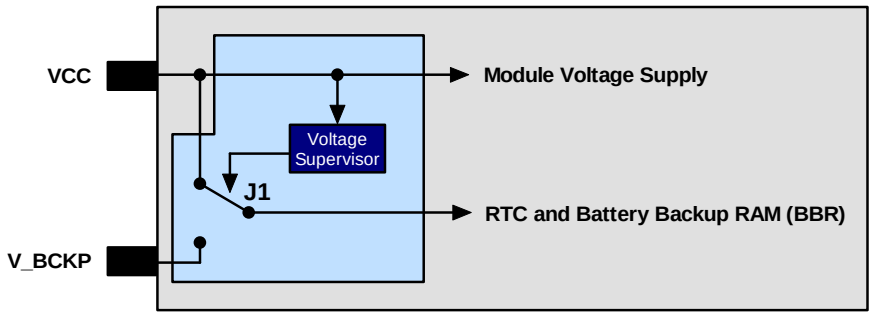


Figure 2: Backup Battery and Voltage

2.1.1.3 VDD_USB - USB Interface Power Supply

VDD_USB supplies the I/Os of the USB interface. If the USB interface is not used, the **VDD_USB** pin must be connected to GND. For more information regarding the correct handling of **VDD_USB** see section 2.3.2.1

2.1.2 Power Modes

u-blox 5 technology offers power optimized architecture with built-in autonomous power saving functions. The receiver uses Autonomous Power Management to minimize the power consumption at any given time. Furthermore, the software shuts down the clock supply to unused peripheral on-chip blocks.

2.1.3 V_ANT

LEA-5 modules supporting active antenna supply and supervision use the pin **V_ANT** to supply the active antenna. Use a 10R resistor in front of **V_ANT**[1]. See chapter 2.9.

[1] Only applies to LEA-5 modules supporting active antenna supply and supervision.

2.2 System Functions

2.2.1 EXTINT - External Interrupt Pin

EXTINT0 is an external interrupt pin. It is used for the time mark function on LEA-5T and will be used in future LEA-5 releases for wake-up functions in low-power modes.

2.2.2 System Monitoring

The u-blox 5 GPS and GALILEO Receiver provides System Monitoring functions that allow the operation of the embedded processor and associated peripherals to be supervised. These System Monitoring functions are being output as part of the UBX protocol, class 'MON'.

Please refer to the *u-blox 5 Protocol Specification [1]*. For more information on UBX messages, serial interfaces for design analysis and individual system monitoring functions.

2.3 Interfaces

2.3.1 Serial

UART 1 (**RxD1/TxD1**) is the default serial interface. It supports data rates from 4.8 to 230.4 kBit/s. The signal output levels are 0 V to VCC (or VDDIO where available). An interface based on RS232 standard levels (+/- 12 V) can be realized using level shifters such as Maxim MAX3232.

☞ The **RxD1** has fixed input voltage thresholds, which do not depend on **VCC** (see *LEA-5 Data Sheet* [3]). Leave open if unused.

Hardware handshake signals and synchronous operation are not supported.

For the default settings see the *LEA-5 Data Sheet* [3].

2.3.2 USB

The u-blox 5 USB interface supports the full-speed data rate of 12 Mbit/s.

2.3.2.1 USB external components

The USB interface requires some external components in order to implement the physical characteristics required by the USB 2.0 specification. These external components are shown in Figure 3 and listed in Table 3.

In order to comply with USB specifications, VBUS must be connected through a LDO (U1) to pin **VDD_USB** of the module.

If the USB device is **self-powered** it is possible that the power supply (VCC) is shut down and the Baseband-IC core is not powered. Since VBUS is still available, it still would be signaled to the USB host that the device is present and ready to communicate. This is not desired and thus the LDO (U1) should be disabled using the enable signal (EN) of the VCC-LDO or the output of a voltage supervisor. Depending on the characteristics of the LDO (U1) it is recommended to add a pull-down resistor (R11) at its output to ensure **VDD_USB** is not floating if LDO (U1) is disabled or the USB cable is not connected i.e. VBUS is not supplied.

If the device is **bus-powered**, LDO (U1) does not need an enable control.

Table 2 lists the present availability of USB on LEA-5 modules. Check the **CFG_COM0** configuration pin (available with LEA-5Q and LEA-5M) to select between Self and Bus Powered modes. For more information on configuration see the *LEA-5 Data Sheet* [3].

	Bus Powered	Self Powered
LEA-5H	•[2]	•
LEA-5S	P	×
LEA-5A	P	×
LEA-5Q	P	•
LEA-5M	P	•
LEA-5T	•	•

•= Supported
×= Not supported
P= Planned availability Q1/09

Table 2: USB availability on LEA-5 modules

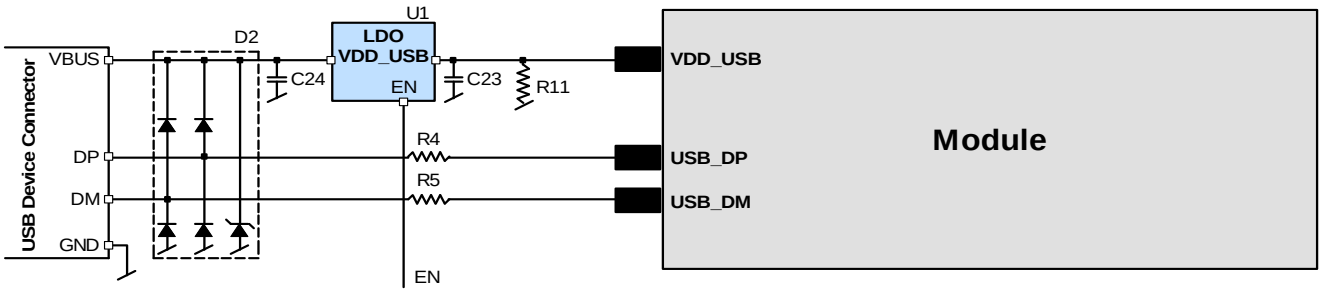


Figure 3: USB Interface

Name	Component	Function	Comments
U1	LDO	Regulates VBUS (4.4 …5.25 V) down to a voltage of 3.3 V).	Almost no current requirement (~1 mA) if the GPS receiver is operated as a USB self-powered device, but if bus-powered LDO (U1) must be able to deliver the maximum current of ~150 mA. A low-cost DC/DC converter such as LTC3410 from Linear Technology may be used as an alternative.
C23, C24	Capacitors		Required according to the specification of LDO U1
D2	Protection diodes	Protect circuit from overvoltage / ESD when connecting.	
R4, R5	Serial termination resistors	Establish a full-speed driver impedance of 28…44 Ohms	A value of 27 Ohms is recommended.
R11	Resistor	Ensures stable signal at **VDD_USB.**	

Table 3: Summary of USB external components

2.3.3 Display Data Channel (DDC)

A DDC interface (**SDA2** / **SCL2**) is available for communication with the host. Pins **SDA2** and **SCL2** have internal pull-ups.

[2] Supported with Firmware V 4.01 and above.

No pull-up resistors are required if the module is used as a DDC/I²C slave (see Figure 4).

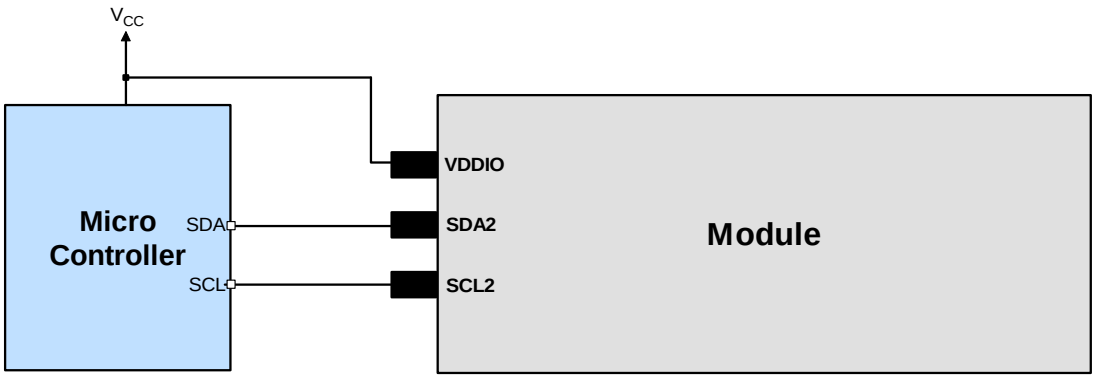


Figure 4: Connecting Module as DDC Slave

☞ No Master Mode: External memory is not supported at this time.

2.3.4 Synchronous Peripheral Interface (SPI)

The SPI interface allows to interface to a host CPU. In slave mode a single chip select signal enables communication with the host.

☞ No Master Mode: External memory is not supported at this time.

2.4 I/O Pins

2.4.1 RESET_N

As with ANTARIS 4 versions, LEA-5 modules come equipped with a **RESET_N** pin. Driving the signal low at **RESET_N** activates a hardware reset of the system. Unlike LEA-4x modules, **RESET_N** is not an I/O with LEA-5. It is only an input and will not reset external circuitry.

Use components with open drain output (i.e. with buffer or voltage supervisor).

There is an internal pull up resistor of 3k3 to VCC inside the module that requires that the reset circuitry can deliver enough current (e.g. 1mA).

RESET_N is provided with LEA-5 modules to provide Reset compatibility with ANTARIS 4 versions. Future LEA models may not include this pin and it is therefore not recommended to use it. The preferred option for executing a hardware reset is to send software commands (CFG-RST).

Do not drive **RESET_N** high.

2.4.2 EXTINT0

EXTINT0 is an external interrupt pin with fixed input voltage thresholds independent of VCC (see the *LEA-5 Data Sheet* [3]). Leave open if unused.

2.4.3 AADET0_N

AADET0_N is an input pin and is used to report whether an external circuit has detected a external antenna or not. Low means antenna has been detected. High means no external antenna has been detected.

See chapter 2.9.5 for an implementation example.

2.4.4 Configuration Pins (CFG_COM0, CFG_COM1, CFG_GPS0)

ROM-based modules provide up to 3 pins (**CFG_COM0, CFG_COM1**, **CFG_GPS0**) for boot-time configuration. These become effective immediately after start-up. Once the module has started, the configuration settings can be modified with UBX configuration messages. The modified settings remain effective until power-down or reset. If these settings have been stored in battery-backup RAM, then the modified configuration will be retained, as long as the backup battery supply is not interrupted.

Some configuration pins are shared with other functions, e.g. SPI. During start-up, the module reads the state of the configuration pins. Afterwards the other functions can be used.

For more information about settings and messages see the *LEA-5 Data Sheet* [3].

2.5 Design-In

This section provides a Design-In Checklist as well as Reference Schematics for new designs with u-blox 5. For migration of existing ANTARIS®4 product designs to u-blox 5 please refer to *Appendix A*.

2.5.1 Schematic Design-In Checklist for LEA-5

Designing-in a LEA-5 GPS/GALILEO receiver is easy especially when a design is based on the reference design in the Hardware Integration Manual. Nonetheless, it pays to do a quick sanity check of the design. This section lists the most important items for a simple design check. The Layout Design-In Checklist also helps to avoid an unnecessary respin of the PCB and helps to achieve the best possible performance.

☞ It is highly recommended to follow the Design-In Checklist when developing any u-blox 5 GPS/GALILEO applications. This can significantly reduce development time and costs.

Have you chosen the optimal module?

LEA-5 modules have been intentionally designed to allow GPS/GALILEO receivers to be optimally tailored to specific applications. Changing between the different variants is easy.

- ❑ Do you need Kick-start performance – Then choose a LEA-5**H**, LEA-5**S,** or LEA-5**Q**.
- ❑ Do you want to be able to upgrade the firmware or to permanently save configuration settings? Then you will have to use a Programmable receiver module: choose a LEA-5**H**.
- ❑ Do you need USB – Then choose a LEA-5**H**, LEA-5**M**, or LEA-5**Q**. Please note that LEA-5**S**, and LEA-5**A** do not yet support USB. See Section 2.3.2 for more information.
- ❑ Do you need Precision Timing – Then choose a LEA-5**T**.

Check Power Supply Requirements and Schematic:

- ❑ Is the power supply within the specified range?
- ❑ Is the voltage **VDDUSB** within the specified range?
- ❑ Compare the peak current consumption of LEA-5 with the specification of your power supply.
- ❑ GPS receivers require a stable power supply, avoid ripple on **VCC** (<50mVpp)

Backup Battery

- ❑ For achieving a minimal Time To First Fix (TTFF) after a power down, make sure to connect a backup battery to **V_BCKP.**

Antenna

- ❑ The total noise figure should be well below 3dB.
- ❑ If a patch antenna is the preferred antenna, choose a patch of at least 15x15mm. Designs using smaller antennas require aiding.
- ❑ Make sure the antenna is not placed close to noisy parts of the circuitry. (e.g. micro-controller, display, etc.)
- ❑ For active antennas add a 10R resistor in front of **V_ANT**[3] input for short circuit protection or use the antenna supervisor circuitry.

Schematic

- ❑ If required, does your schematic allow using different LEA-5 variants?
- ❑ Don't drive **RESET_N** high!
- ❑ Plan use of 2nd interface (Testpoints on serial port, DDC or USB) for firmware updates or as a service connector.

[3] Only available with LEA-5-H, LEA-5S, LEA-5A, LEA-5T

2.6 LEA-5 Design

For a minimal Design with LEA-5 the following functions and pins need to be considered:

- Connect the Power supply to **VCC.**
- **VDDUSB:** Connect the USB power supply to a LDO before feeding it to **VDDUSB** and **VCC**. Or connect to GND if USB is not used.
- Assure a optimal ground connection to all ground pins of the LEA module
- Connect the antenna to **RF_IN** over a matching 50 Ohm micro strip and define the antenna supply (**V_ANT**)[4] for active antennas (internal or external power supply)
- Choose the required serial communication interface (USART, USB or DDC) and connect the appropriate pins to your application
- If you need Hot- or Warmstart in your application, connect a Backup Battery to **V_BCKP**
- Decide whether **TIMEPULSE** or **RESET_N** options are required in your application and connect the appropriate pins on your module

2.6.1 LEA-5 Passive Antenna Design (LEA-5-H, LEA-5S, LEA-5A, LEA-5T)

This is a minimal setup for a PVT GPS/GALILEO receiver.

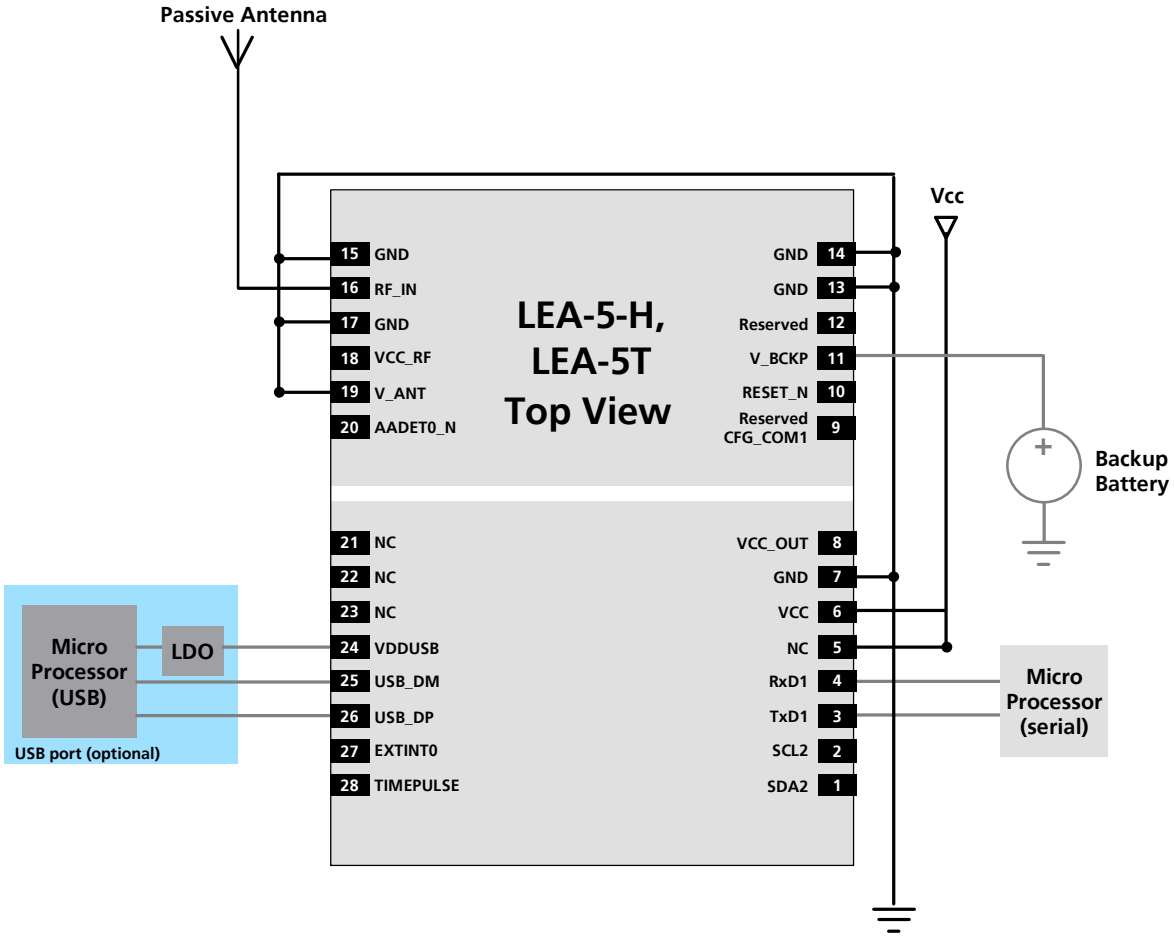


Figure 5: Passive Antenna Design for LEA-5-H, LEA-5T Receivers

[4] Only available with LEA-5-H, LEA-5S, LEA-5A, LEA-5T

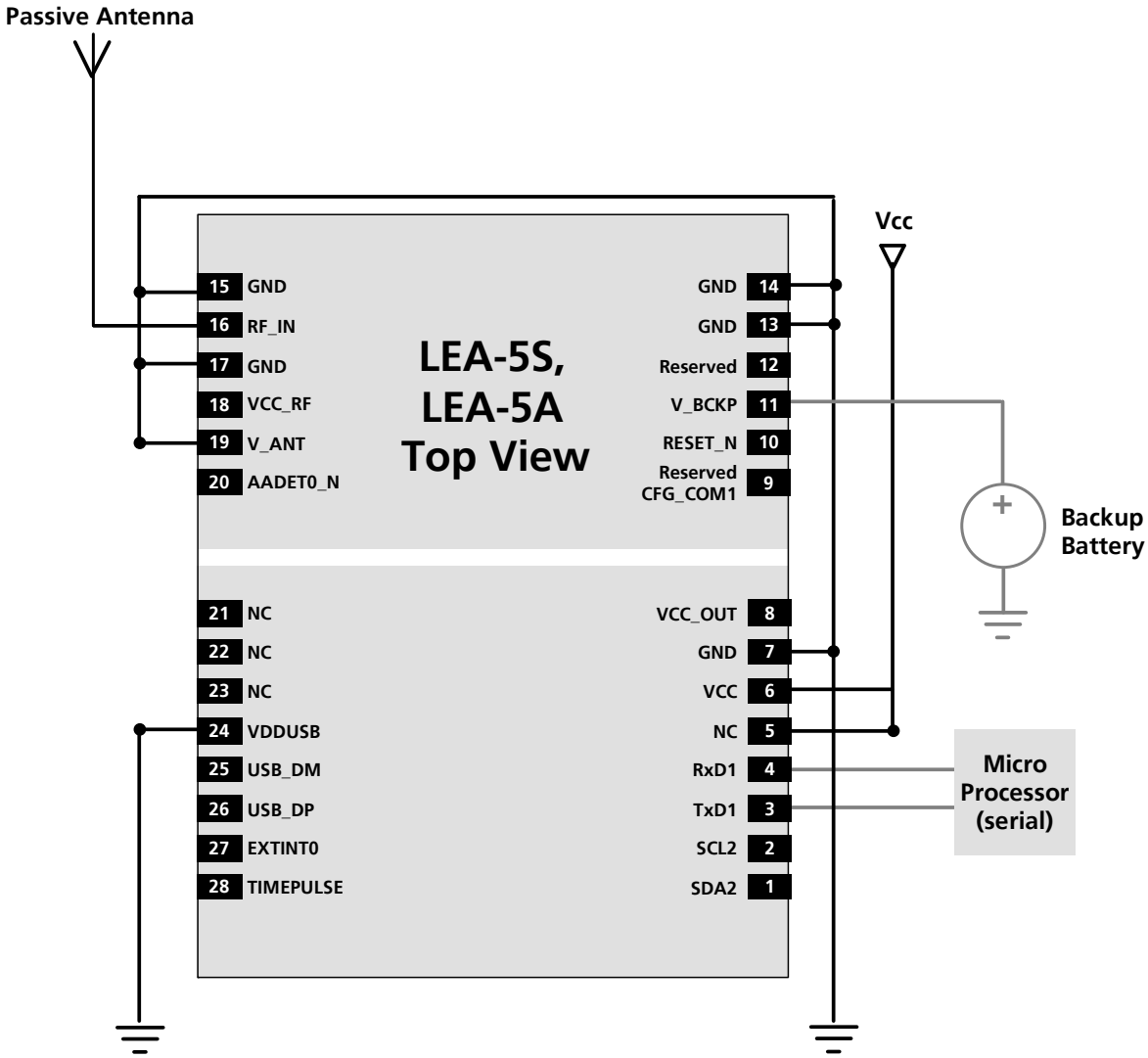


Figure 6: Passive Antenna Design for LEA-5S, LEA-5A Receivers

Function	PIN	I/O	Description	Remarks
Power				
VCC	6	I	Supply Voltage	Provide clean and stable supply.
GND	7, 13-15, 17	I	Ground	Assure a good **GND** connection to all **GND** pins of the module, preferably with a large ground.
VCC_OUT	8	O		Connected to VCC. Leave open if not used.
V_BCKP	11	I	Backup voltage supply	It's recommended to connect a backup battery to **V_BCKP** in order to enable Warm and Hot Start features on the receivers. Otherwise connect to **GND** (or **VCC**).
VDDUSB	24	I	USB Power Supply	To use the USB interface connect this pin to 3.0 – 3.6V derived from VBUS. If no USB serial port used connect to GND.
Antenna				
RF_IN	16	I	GPS/GALILEO signal input from antenna	Use a controlled impedance transmission line of 50 Ohm to connect to RF_IN. Don't supply DC through this pin. Use **V_ANT** pin to supply power.
VCC_RF	18	O	Output Voltage RF section	Can be used to power an external active antenna (**VCC_RF** connected to **V_ANT**). The max power consumption of the Antenna must not exceed the datasheet specification of the module. Leave open if not used.
V_ANT	19	I	Antenna Bias voltage	Connect to **GND** (or leave open) if Passive Antenna is used. If an active Antenna is used, add a 10R resistor in front of **V_ANT** input to the Antenna Bias Voltage or **VCC_RF** for short circuit protection or use the antenna supervisor circuitry.
AADET0_N	20	I	Active Antenna Detect	Input pin for optional antenna supervisor circuitry. Leave open if not used.
Serial Port /USB				
TxD1	3	O	Serial Port 1	Serial port output. Leave open if not used.
RxD1	4	I	Serial Port 1	Serial port input with internal pull-up resistor to VCC. Leave open if not used. ☞ Don't use an external pull up resistor.
USB_DM[5]	25	I/O	USB I/O line	USB2.0 bidirectional communication pin. Leave open if unused. Implementation see Section 2.3.2.
USB_DP[5]	26			
System				
RESET_N	10	I	Hardware Reset (Active Low)	Leave open if not used. Do not drive high.
TIMEPULSE	28	O	Timepulse Signal	Configurable Timepulse signal (one pulse per second by default). Leave open if not used.
EXTINT0	27	I	External Interrupt	External Interrupt Pin. Internal pull-up resistor to **VCC**. Leave open if not used.
CFG_COM1/ Reserved	9	I	Configuration Pin/ Reserved	LEA-5S, LEA-5A: Leave open for default configuration. LEA-5H, LEA-5T: Reserved
SDA2	1	I/O	DDC Pins	DDC Data. Leave open if not used.
SCL2	2			DDC Clock. Leave open if not used.
Reserved	12	I		Leave open, do not drive low.
NC	5			Can be left open, but **connection to VCC is recommended** for compatibility reasons. I/O voltage is always VCC.
NC	21-22		Not Connect	Leave open
NC	23		Not Connect	Leave open

Table 4: Pinout LEA-5-H, LEA-5S, LEA-5A, LEA-5T

[5] Planned availability Q1/09 for LEA-5S and LEA-5A

2.6.2 Passive Antenna Design (LEA-5-Q, LEA-5M)

This is a minimal setup for a PVT GPS/GALILEO receiver.

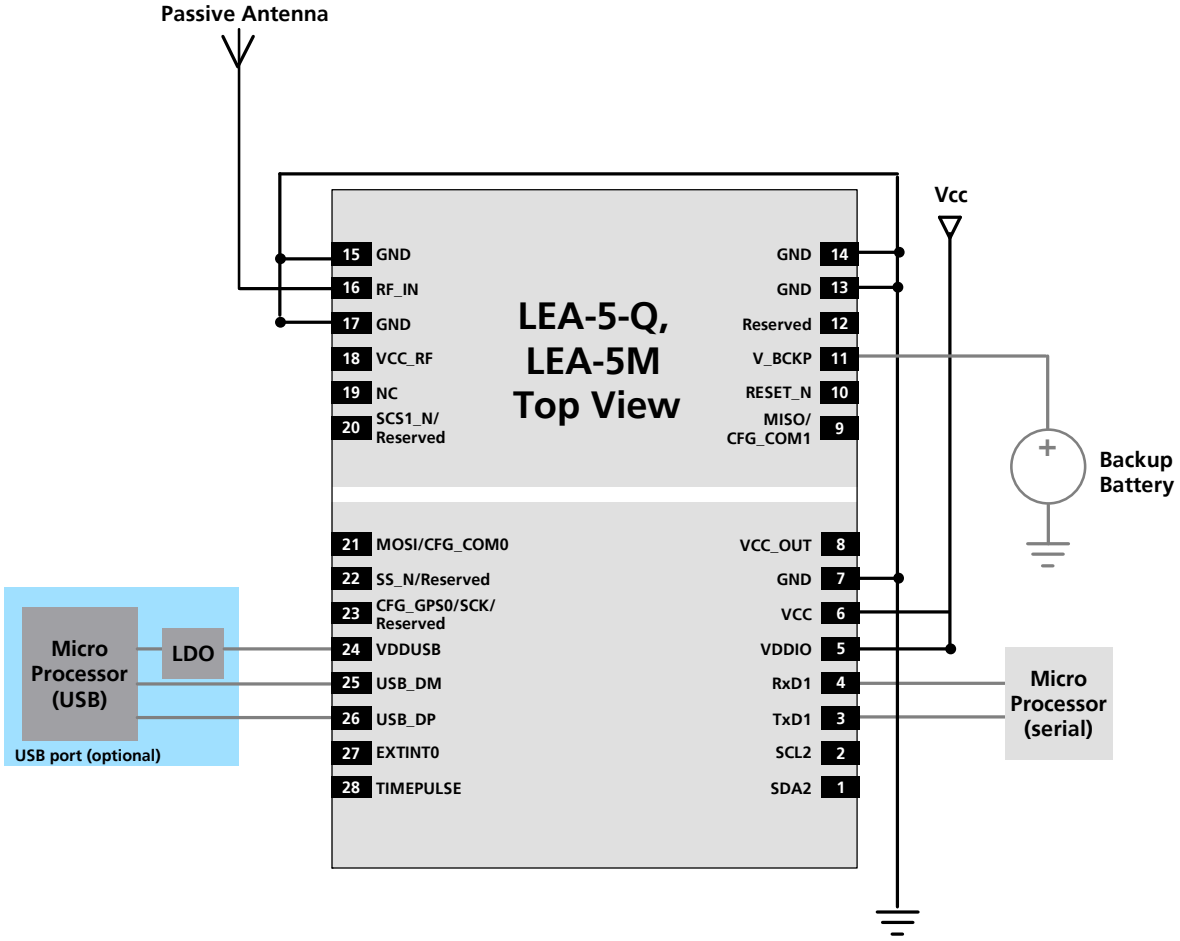


Figure 7: Pinout LEA-5-Q, LEA-5M

Function	PIN	I/O	Description	Remarks
Power				
VCC	6	I	Supply Voltage	Provide clean and stable supply.
GND	7, 13-15, 17	I	Ground	Assure a good **GND** connection to all **GND** pins of the module, preferably with a large ground plane.
VCC_OUT	8	O		Connected to VCC. Leave open if not used.
V_BCKP	11	I	Backup voltage supply	It's recommended to connect a backup battery to **V_BCKP** in order to enable Warm and Hot Start features on the receivers. Otherwise connect to **GND** (or VCC).
VDDUSB	24	I	USB Power Supply	To use the USB interface connect this pin to 3.0-3.6V derived from VBUS. If no USB serial port used connect to GND.
VDDIO	5	I	I/O Voltage	Defines the I/O voltage. Do not leave open.
Antenna				
RF_IN	16	I	GPS/GALILEO signal input from antenna	Use a controlled impedance transmission line of 50 Ohm to connect to RF_IN. Antenna bias voltage for active antennas is not provided on the **RF_IN** pin. If an active Antenna is used an external voltage is required (see *Section 2.9.3)*.
VCC_RF	18	O	Output Voltage RF section	Leave open
Serial Port /USB				
TxD1	3	O	Serial Port 1	Serial port output. Leave open if not used.
RxD1	4	I	Serial Port 1	**Serial port input with internal pull-up resistor to** VCC**. Leave open if not used.** ☞ Don't use an external pull up resistor.
USB_DM	25	I/O	USB I/O line	USB2.0 bidirectional communication pin. Leave open if unused. Implementation see Section 2.3.2.
USB_DP	26			
System				
RESET_N	10	I	Hardware Reset (Active Low)	Leave open if not used. Do not drive high.
TIMEPULSE	28	O	Timepulse Signal	Configurable Timepulse signal (one pulse per second by default). Leave open if not used.
EXTINT0	27	I	External Interrupt	External Interrupt Pin. Internal pull-up resistor to **VCC**. Leave open if not used.
SDA2	1	I/O	DDC Pins	DDC Data. Leave open, if not used.
SCL2	2			DDC Clock. Leave open, if not used.
Reserved	12	I		Leave open, do not drive low.
NC	19		Not Connected	Leave open.
SCS1_N/ Reserved	20	O	SPI	LEA-5Q: SPI Chip Select. Leave open if not used. LEA-5M: Leave open.
MISO/ CFG_COM1	9	I/O	SPI Configuration Pin	LEA-5Q: SPI MISO. Leave open, if not used. LEA-5Q/LEA-5M: Leave open for default configuration.
MOSI/ CFG_COM0	21	I/O	SPI Configuration Pin	LEA-5Q: SPI MOSI. Leave open, if not used. LEA-5Q/LEA-5M: Leave open for default configuration.
SS_N/ Reserved	22	I	SPI Reserved	LEA-5Q: SPI Slave Select. Leave open, if not used. LEA-5M: Leave open.
SCK/CFG_GPS/ Reserved	23	I/O	SPI/Power Mode	LEA-5Q: SPI Clock / Power Mode Configuration Pin. Leave open, if not used. LEA-5M: Leave open.

Table 5: Pinout LEA-5-Q, LEA-5M

2.7 Layout Design-In Checklist

Follow this checklist for the Layout design to get an optimal GPS performance.

Layout optimizations (*Section 2.8*)

- ❑ Is the GPS module placed according to the recommendation in *Section 2.8.3*?
- ❑ Has the Grounding concept been followed (see *Section 2.8.4*)?
- ❑ Has the micro strip been kept as short as possible?
- ❑ Add a ground plane underneath the GPS module to reduce interference.
- ❑ For improved shielding, add as many vias as possible around the micro strip, around the serial communication lines, underneath the GPS module etc.

Calculation of the micro strip (*Section 2.8.5*)

- ❑ The micro strip must be 50 Ohms and be routed in a section of the PCB where minimal interference from noise sources can be expected.
- ❑ In case of a multi-layer PCB, use the thickness of the dielectric between the signal and the 1st **GND** layer (typically the 2nd layer) for the micro strip calculation.
- ❑ If the distance between the micro strip and the adjacent **GND** area (on the same layer) does not exceed 5 times the track width of the micro strip, use the "Coplanar Waveguide" model in AppCad to calculate the micro strip and not the "micro strip" model.

2.8 Layout

This section provides important information for designing a reliable and sensitive GPS/GALILEO system.

GPS signals at the surface of the Earth are about 15dB below the thermal noise floor. Signal loss at the antenna and the RF connection must be minimized as much as possible. When defining a GPS receiver layout, the placement of the antenna with respect to the receiver, as well as grounding, shielding and jamming from other digital devices are crucial issues and need to be considered very carefully.

2.8.1 Footprint

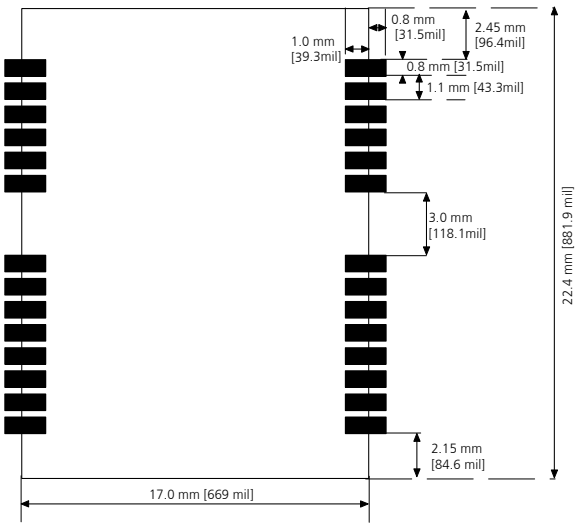


Figure 8: Recommended footprint

2.8.2 Paste Mask

Figure 9 shows the recommended positioning of the Paste Mask, the Copper and Solder masks, as well as the step stencil. These are recommendations only and not specifications. Note that the Copper and Solder masks have the same size and position.

To improve the wetting of the half vias, reduce the amount of solder paste under the module and increase the volume outside of the module by defining the dimensions of the paste mask to form a T-shape (or equivalent) extending beyond the Copper mask as shown in Figure 9. In addition, use a step stencil covering the entire area of the module and beyond the paste mask to increase the volume of solder paste here. The solder paste at the step stencil should have a total thickness of 175 to 200 µm.

If a step stencil is not used it is still advisable to increase the volume of solder paste **outside** the module to attain the desired level of wetting. This must be done by modifying the shape of the paste mask outside the module, to allow for the increased volume of solder paste.

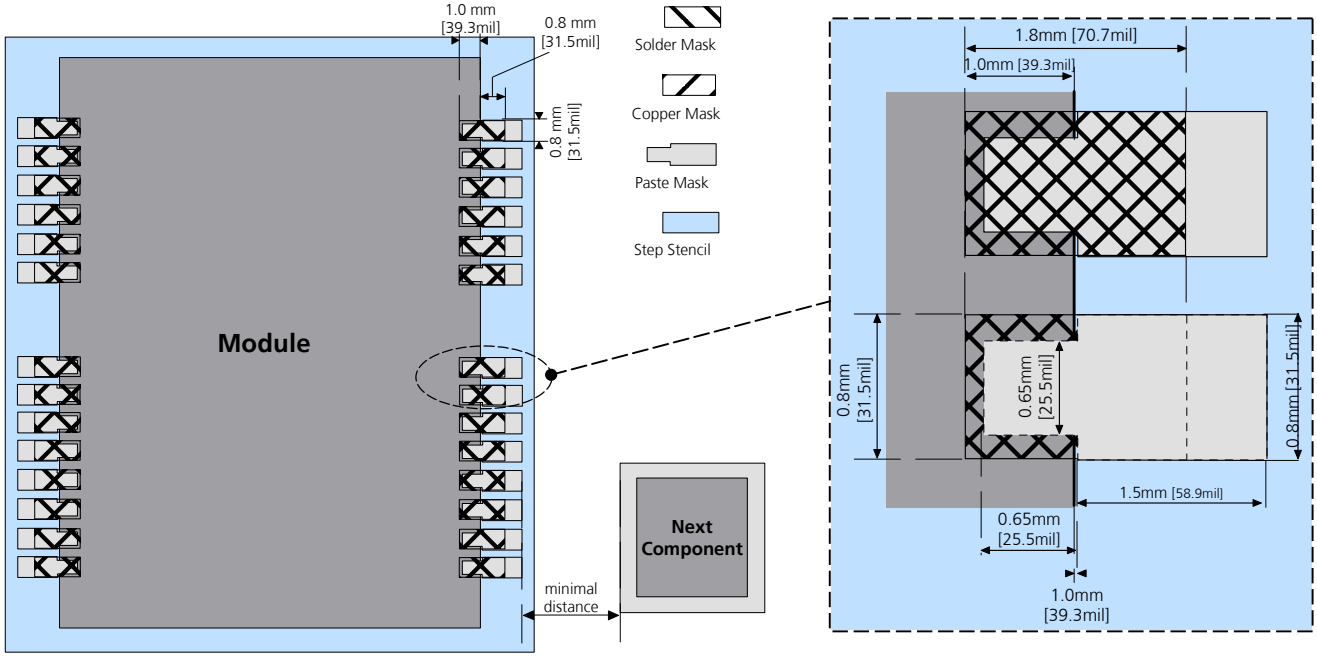


Figure 9: Recommendations for copper, solder and paste masks with enlargement

☞ The paste mask outline needs to be considered when defining the minimal distance to the next component.

☞ The exact geometry, distances, stencil thicknesses, step heights and solder paste volumes must be adapted to the specific production processes (e.g. soldering etc.) of the customer.

2.8.3 Placement

A very important factor in achieving maximum GPS and GALILEO performance is the placement of the receiver on the PCB. The connection to the antenna must be as short as possible to avoid jamming into the very sensitive RF section.

Make sure that RF critical circuits are clearly separated from any other digital circuits on the system board. To achieve this, position the receiver digital part towards your digital section of the system PCB. Care must also be exercised with placing the receiver in proximity to circuitry that can emit heat. The RF part of the receiver is very sensitive to temperature and sudden changes can have an adverse impact on performance.

The RF part of the receiver is a temperature sensitive component. Avoid high temperature drift and air vents near the receiver.

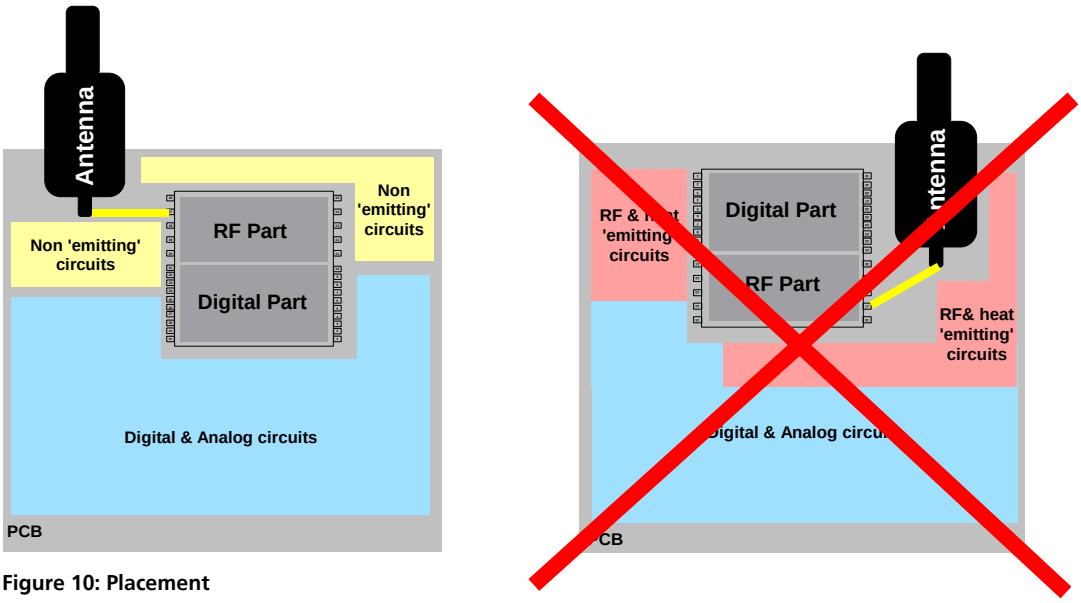


Figure 10: Placement

2.8.4 Antenna Connection and Grounding Plane Design

u-blox 5 modules can be connected to passive patch or active antennas. The RF connection is on the PCB and connects the **RF_IN** pin with the antenna feed point or the signal pin of the connector, respectively. *Figure 11* illustrates connection to a typical five-pin RF connector. One can see the improved shielding for digital lines as discussed in *Appendix* D.3. Depending on the actual size of the ground area, additional vias should be placed in the outer region. In particular, the edges of the ground area should be terminated with a dense line of vias.

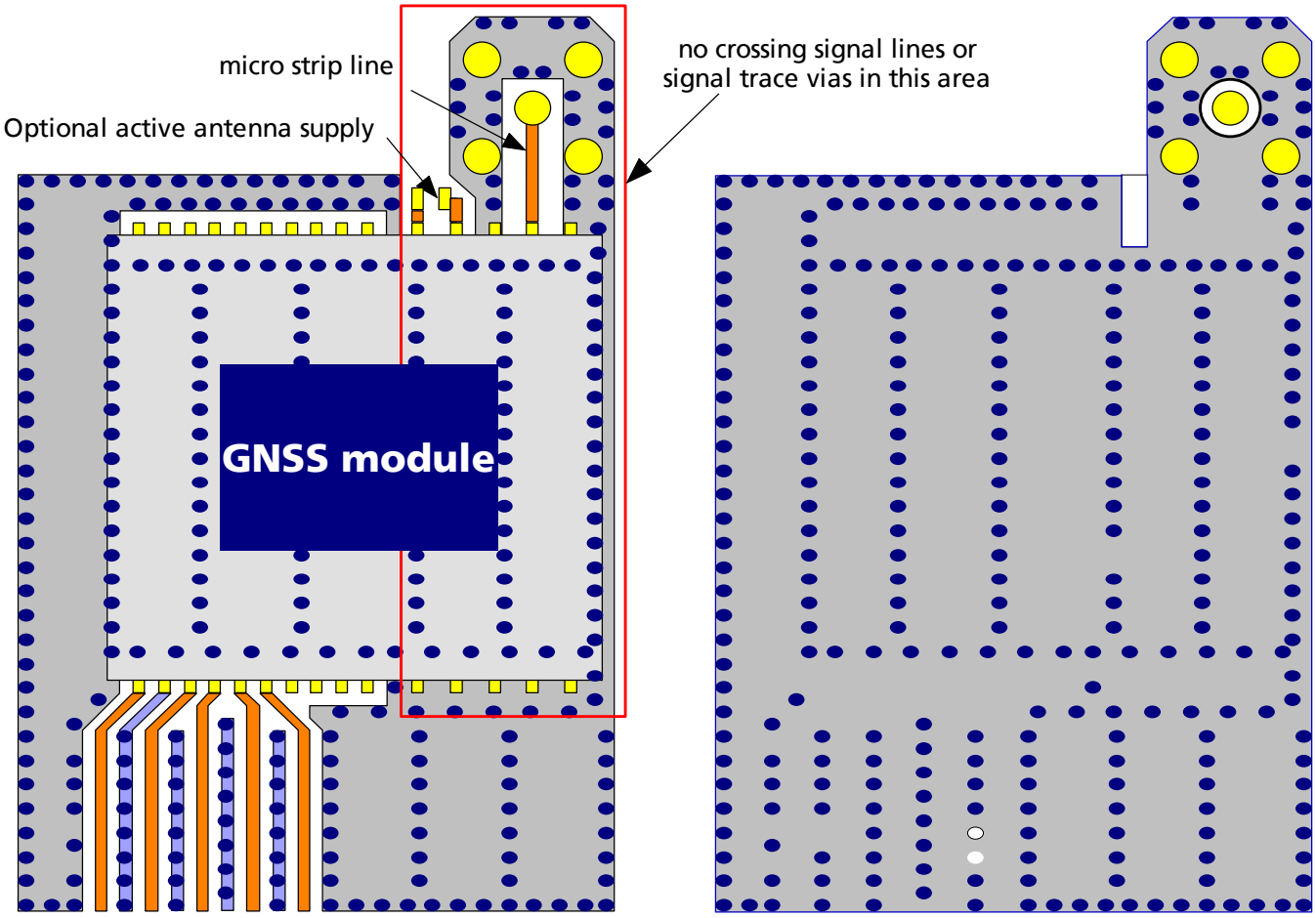


Figure 11: Recommended layout

As seen in *Figure 11,* an isolated ground area is created around and below the RF connection. This part of the circuit MUST be kept as far from potential noise sources as possible. Make certain that no signal lines cross, and that no signal trace vias appear at the PCB surface within the area of the red rectangle. The ground plane should also be free of digital supply return currents in this area. On a multi layer board, the whole layer stack below the RF connection should be kept free of digital lines. This is because even solid ground planes provide only limited isolation.

The impedance of the antenna connection has to match the 50 Ohm impedance of the receiver. To achieve an impedance of 50 Ohms, the width W of the micro strip has to be chosen depending on the dielectric thickness H, the dielectric constant ε_r of the dielectric material of the PCB and on the build-up of the PCB (see *Section 2.8.5*). *Figure 12* shows two different builds: A 2 Layer PCB and a 4 Layer PCB. The reference ground plane is in both designs on layer 2 (red). Therefore the effective thickness of the dielectric is different.

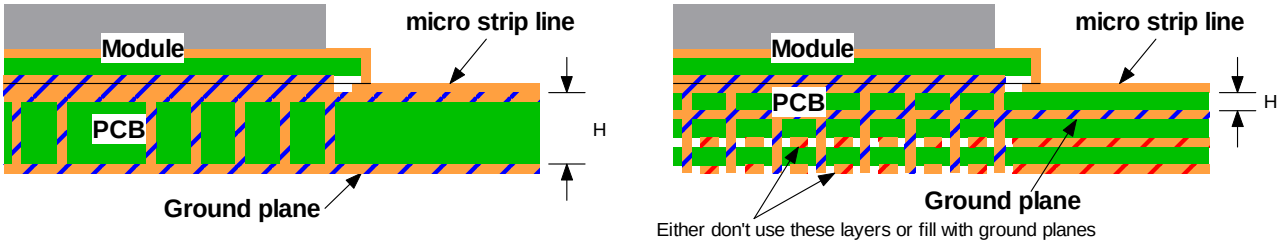
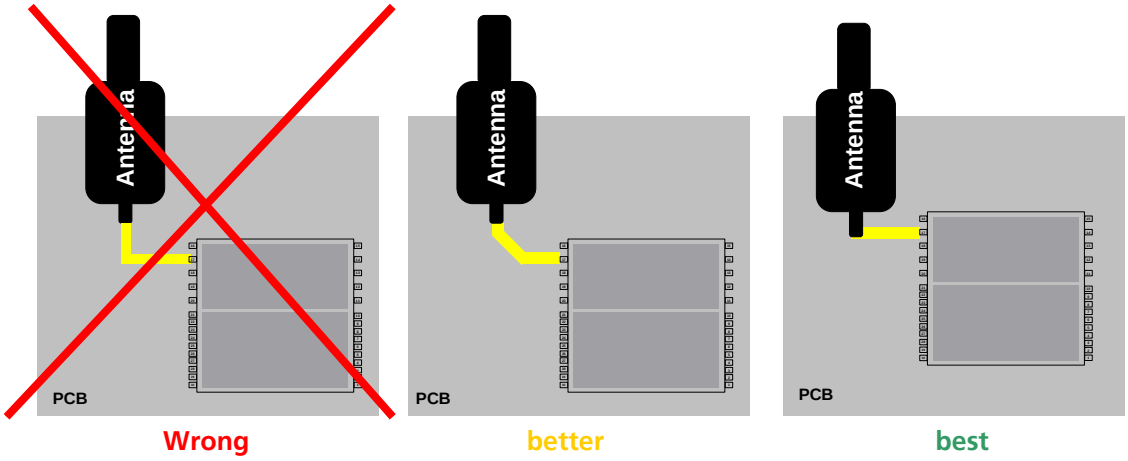


Figure 12: PCB build-up for Micro strip line. Left: 2-layer PCB, right: 4-layer PCB

General design recommendations:

- The length of the micro strip line should be kept as short as possible. Lengths over 2.5 cm (1 inch) should be avoided on standard PCB material and without additional shielding.
- Distance between micro strip line and ground area on the top layer should at least be as large as the dielectric thickness.
- Routing the RF connection close to digital sections of the design should be avoided.
- To reduce signal reflections, sharp angles in the routing of the micro strip line should be avoided. Chamfers or fillets are preferred for rectangular routing; 45-degree routing is preferred over Manhattan style 90-degree routing.



- Routing of the RF-connection underneath the receiver should be avoided. The distance of the micro strip line to the ground plane on the bottom side of the receiver is very small (some 100 µm) and has huge tolerances (up to 100%). Therefore, the impedance of this part of the trace cannot be controlled.
- Use as many vias as possible to connect the ground planes.
- In order to avoid reliability hazards, the area on the PCB under the receiver should be entirely covered with solder mask. Vias should not be open.

2.8.5 Antenna Micro Strip

There are many ways to design wave-guides on printed circuit boards. Common to all is that calculation of the electrical parameters is not straightforward. Freeware tools like AppCAD from Agilent or TXLine from Applied Wave Research, Inc. are of great help. They can be downloaded from *www.agilent.com* and *www.mwoffice.com*.

The micro strip is the most common configuration for printed circuit boards. The basic configuration is shown in *Figure 13* and *Figure 14*. As a rule of thumb, for a FR-4 material the width of the conductor is roughly double the thickness of the dielectric to achieve 50 Ohms line impedance.

For the correct calculation of the micro strip impedance, one does not only need to consider the distance between the top and the first inner layer but also the distance between the micro strip and the adjacent GND plane on the same layer

☞ Use the Coplanar Waveguide model for the calculation of the micro strip.

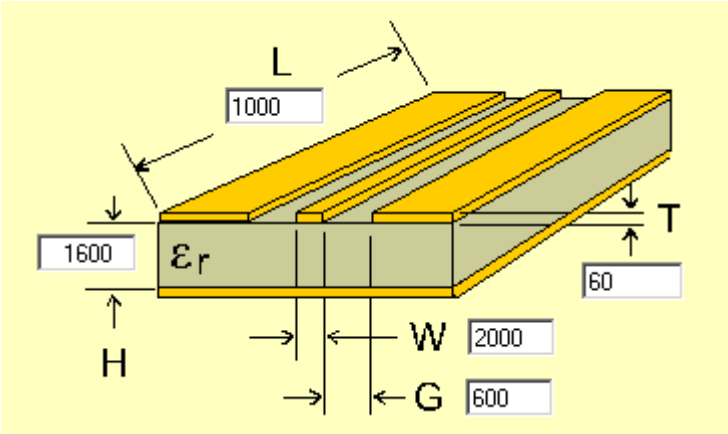


Figure 13: Micro strip on a 2-layer board (Agilent AppCAD Coplanar Waveguide)

Figure 13 shows an example of a 2-layer FR4 board of 1.6 mm thickness and a 35µm (1 once) copper cladding. The thickness of the micro strip is comprised of the cladding (35µm) plus the plated cupper (typically 25µm). *Figure 14* depicts an example of a multi layer FR4 board with 18µm (½ once) cladding and 180µ dielectric between layer 1 and 2.

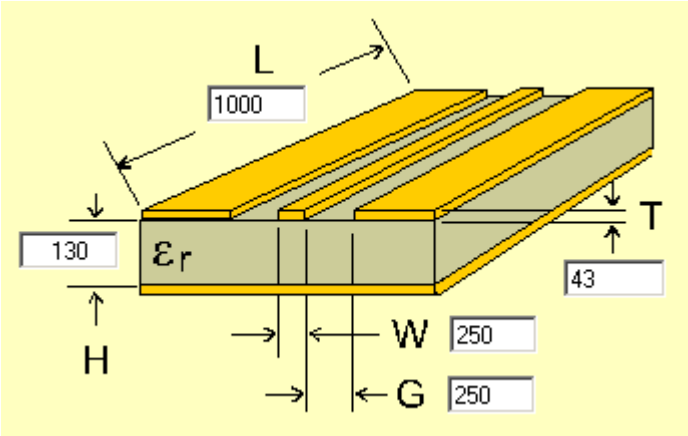


Figure 14: Micro strip on a multi layer board (Agilent AppCAD Coplanar Waveguide)

2.9 Antenna and Antenna Supervisor

u-blox 5 modules receive L1 band signals from GPS and GALILEO satellites at a nominal frequency of 1575.42 MHz. The RF signal is connected to the **RF_IN** pin.

u-blox 5 modules can be connected to passive or active antennas.

☞ For u-blox 5 receivers, the total preamplifier gain (minus cable and interconnect losses) must not exceed 50 dB. Total noise figure should be below 3 dB.

The u-blox 5 Technology supports either a short circuit protection of the active antenna or an active antenna supervisor circuit (open and short circuit detection). For further information refer to *Section 2.9.2).*

2.9.1 Passive Antenna

A design using a passive antenna requires more attention regarding the layout of the RF section. Typically a passive antenna is located near electronic components; therefore care should be taken to reduce electrical 'noise' that may interfere with the antenna performance. Passive antennas do not require a DC bias voltage and can be directly connected to the RF input pin **RF_IN**. Sometimes, they may also need a passive matching network to match the impedance to 50 Ohms.

☞ Some passive antenna designs present a DC short to the RF input, when connected. If a system is designed with antenna bias supply AND there is a chance of a passive antenna being connected to the design, consider a short circuit protection.

☞ All u-blox 5 receivers have a built-in LNA required for passive antennas.

2.9.2 Active Antenna (LEA-5-H, LEA-5S, LEA-5A, LEA-5T)

Active antennas have an integrated low-noise amplifier. They can be directly connected to **RF_IN**. If an active antenna is connected to **RF_IN**, the integrated low-noise amplifier of the antenna needs to be supplied with the correct voltage through pin **V_ANT** or an external inductor. Usually, the supply voltage is fed to the antenna through the coaxial RF cable. Active antennas require a power supply that will contribute to the total GPS system power consumption budget with additional 5 to 20 mA typically. Inside the antenna, the DC component on the inner conductor will be separated from the RF signal and routed to the supply pin of the LNA (see Figure 15).

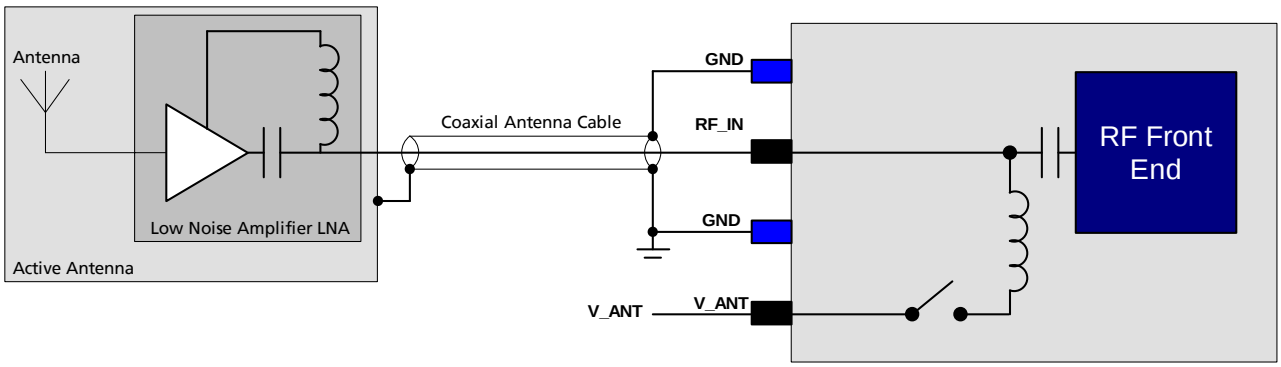


Figure 15: Active antenna biasing

Generally an active antenna is easier to integrate into a system design, as it is less sensitive to jamming compared to a passive antenna. But an active antenna must also be placed far from any noise sources to have good performance.

Antennas should only be connected to the receiver when the receiver is not powered. Do not connect or disconnect the Antenna when the u-blox 5 receiver is running as the receiver calibrates the noise floor on power-up. Connecting the antenna after power-up can result in prolonged acquisition time.

Never feed supply voltage into RF_IN. Always feed via V_ANT or an external inductor .

☞ To test GPS/GALILEO signal reacquisition, it is recommended to physically block the signal to the antenna, rather than disconnecting and reconnecting the receiver.

2.9.3 Active Antenna (LEA-5-Q, LEA-5M)

LEA-5-Q and LEA-5M modules do not provide the antenna bias voltage for active antennas on the **RF_IN** pin. It is therefore necessary to provide this voltage outside the module via an inductor as indicated in Figure 16. u-blox recommends using an inductor from Coilcraft (0402CS-36NX). Alternative parts can be used if the inductor's resonant frequency matches the GPS frequency of 1575.4MHz.

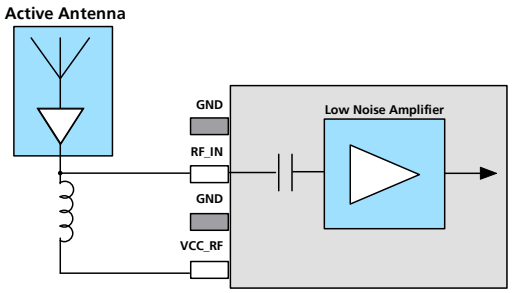


Figure 16: Recommended wiring for active antennas

For optimal performance, it is important to place the inductor as close to the microstrip as possible. Figure 15 illustrates the recommended layout and how it should not be done.

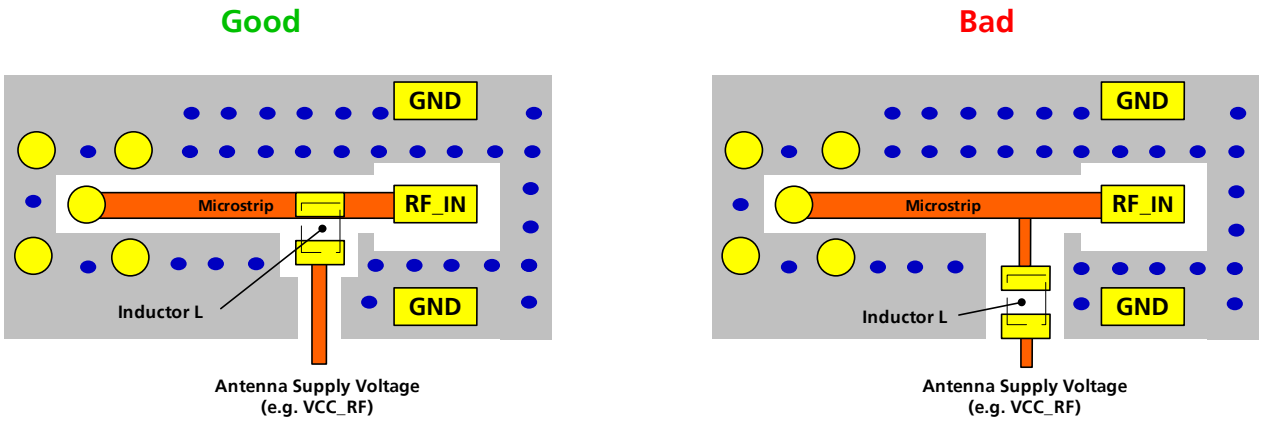


Figure 17: Recommended layout for connecting the antenna bias voltage for LEA-5-Q and LEA-5M

2.9.4 Active Antenna Bias Power (LEA-5-H, LEA-5S, LEA-5A, LEA-5T)

There are two ways to supply the bias voltage to pin **V_ANT**. It can be supplied externally (please consider the datasheet specification) or internally. For Internal supply, the **VCC_RF** output must be connected to **V_ANT** to supply the antenna with a filtered supply voltage. However, the voltage specification of the antenna has to match the actual supply voltage of the u-blox 5 Receiver (e.g. 3.0 V).

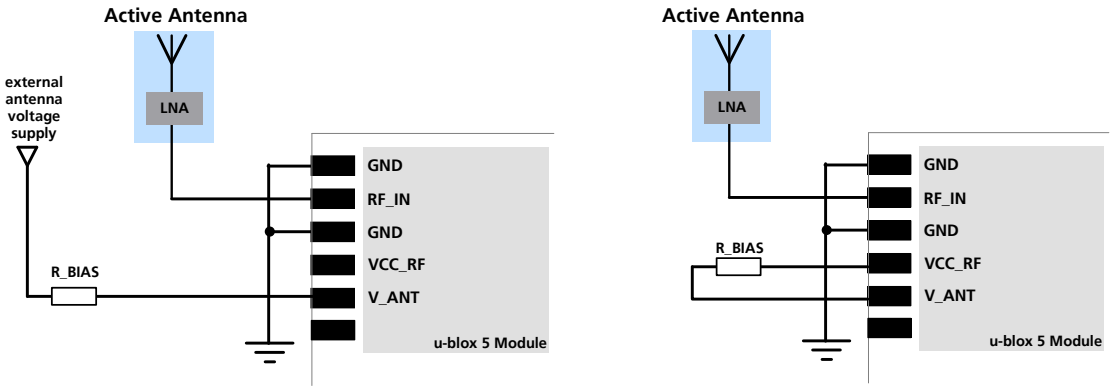


Figure 18: Supplying Antenna bias voltage

Since the bias voltage is fed into the most sensitive part of the receiver, i.e. the RF input, this supply should be virtually free of noise. Usually, low frequency noise is less critical than digital noise with spurious frequencies with harmonics up to the GPS/GALILEO band of 1.575 GHz. Therefore, it is not recommended to use digital supply nets to feed pin **V_ANT**.

An internal switch (under control of the u-blox 5 software) can shutdown the supply to the external antenna whenever it is not needed. This feature helps to reduce power consumption.

2.9.4.1 Short Circuit Protection

If a reasonably dimensioned series resistor **R_BIAS** is placed in front of pin **V_ANT**, a short circuit situation can be detected by the baseband processor. If such a situation is detected, the baseband processor will shut down supply to the antenna. The receiver is by default configured to attempt to reestablish antenna power supply periodically.

☞ To configure the antenna supervisor use the UBX-CFG-ANT message. For further information refer to the *u-blox 5 Protocol Specification [1].*

References	Value	Tolerance	Description	Manufacturer
R_BIAS	10 Ω	± 10%	Resistor, min 0.250 W	

Table 7: Short circuit protection, bill of material

⚠ **Short circuits on the antenna input without limitation of the current can result in permanent damage to the receiver! Therefore, it's recommended to implement an R_BIAS in all risk applications, such as situations where the antenna can be disconnected by the end-user or that have long antenna cables.**

☞ An additional R_BIAS is not required when using a short and open active antenna supervisor circuitry as defined in *Section 2.9.5.1*, as the R_BIAS is equal to R2.

2.9.5 Active Antenna Supervisor (LEA-5-H, LEA-5S, LEA-5A, LEA-5T)

u-blox 5 Technology provides the means to implement an active antenna supervisor with a minimal number of parts. The antenna supervisor is highly configurable to suit various different applications.

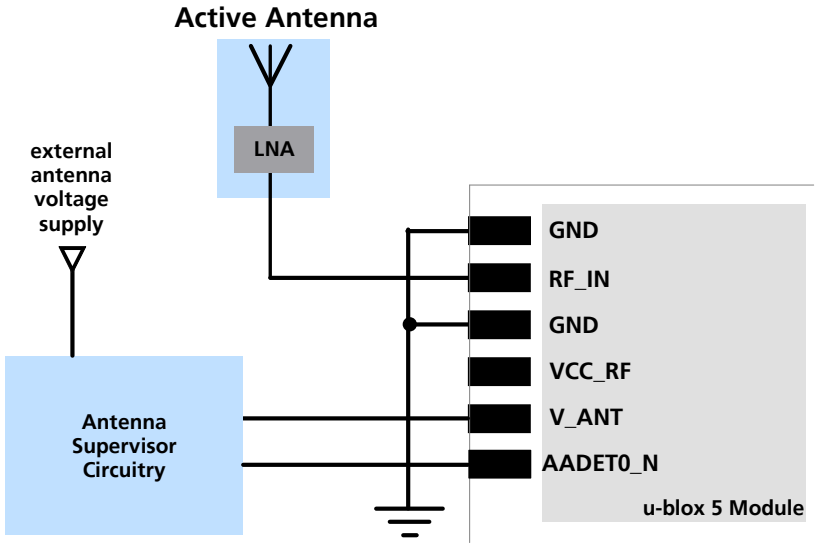


Figure 19: External antenna power supply with full antenna supervisor

2.9.5.1 Short and Open Circuit Active Antenna Supervisor

The Antenna Supervisor can be configured by a serial port message (using only UBX binary message).

When enabled the active antenna supervisor produces serial port messages (status reporting in NMEA and/or UBX binary protocol) which indicates all changes of the antenna circuitry (**disabled** antenna supervisor, antenna circuitry **ok**, **short** circuit, **open** circuit) and shuts the antenna supply down if required.

The active antenna supervisor provides the means to check the active antenna for open and short circuits and to shut the antenna supply off, if a short circuit is detected.

The following state diagram applies. If an antenna is connected, the initial state after power-up is "Active Antenna OK".

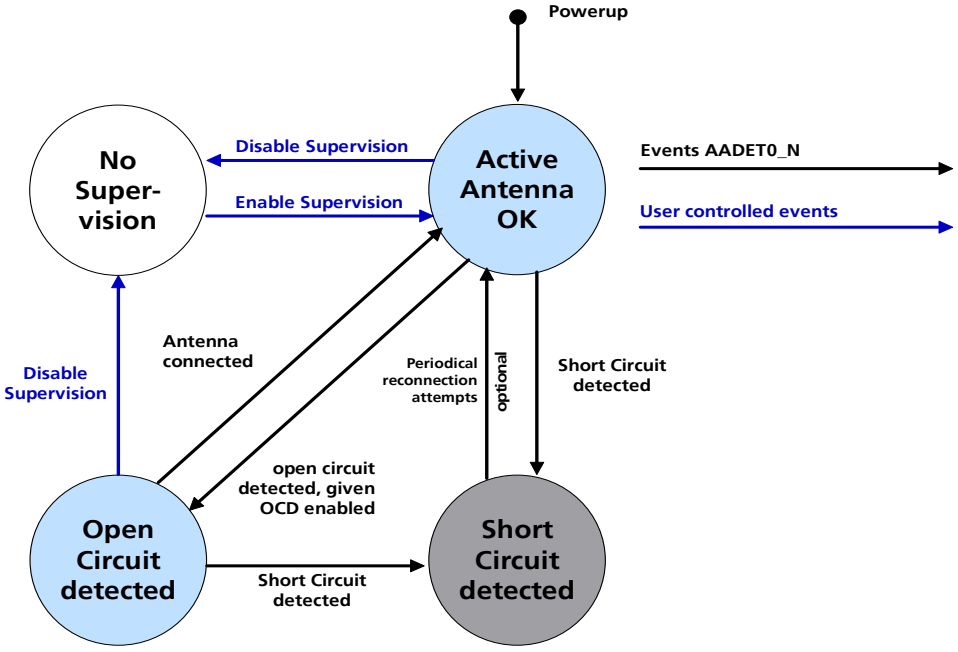


Figure 20: State Diagram of Active Antenna Supervisor

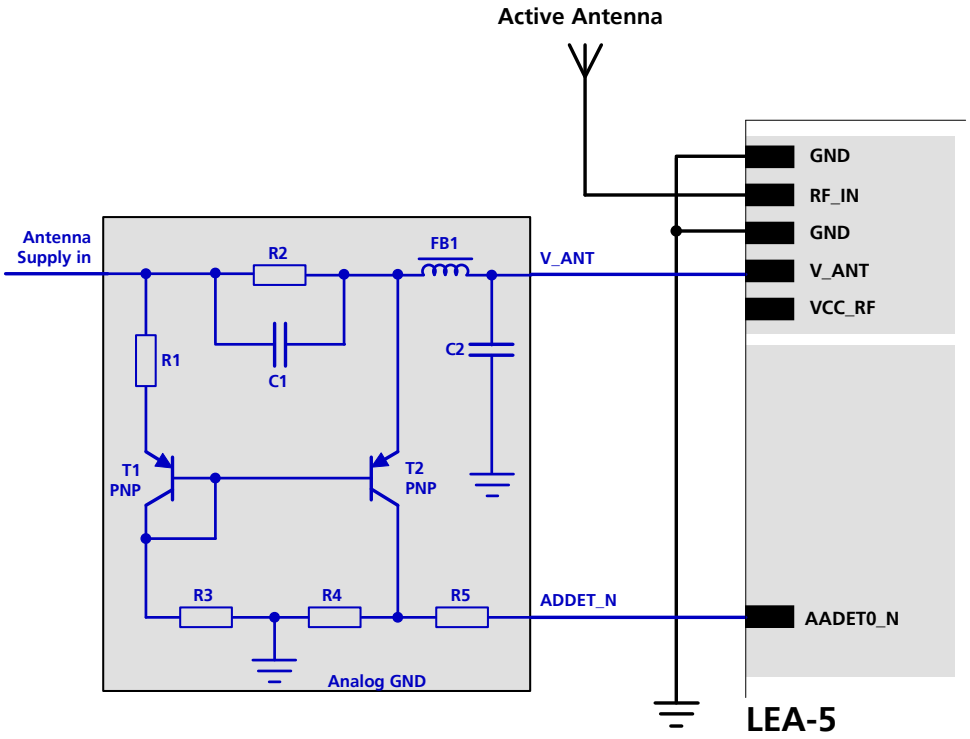


Figure 21: Schematic of open circuit detection

References	Value	Tolerance	Description	Remarks
C1	2.2 µF	± 10%	Capacitor, X7R, min 10 V	
C2	100 nF	± 10%	Capacitor, X7R, min 10 V	
FB1	600 Ω		Ferrite Bead	e.g. Murata BLM18HD601SN1
R1	15 Ω	± 10%	Resistor, min 0.063 W	
R2	10 Ω	± 10%	Resistor, min 0.250 W	
R3, R4	10 kΩ	± 10%	Resistor, min 0.063 W	
R5	33 kΩ	± 10%	Resistor, min 0.063 W	
T1, T2			PNP Transistor BC856B	e.g. Philips Semiconductors[6]

Table 8: Active Antenna Supervisor, bill of material

Firmware supports an active antenna supervisor circuit, which is connected to the pin **AADET0_N**. An example of an open circuit detection circuit is shown in Figure 21. High on **AADET0_N** means that an external antenna is not connected.

Short Circuit Detection (SCD)

A short circuit in the active antenna pulls **V_ANT** to ground. This is detected inside the u-blox 5 module and the antenna supply voltage will be immediately shut down.

☞ Antenna short detection (SCD) and control is enabled by default.

[6] Transistors from other suppliers with comparable electrical characteristics may be used.

Open Circuit Detection (OCD)

The open circuit detection circuit uses the current flow to detect an open circuit in the antenna. The threshold current is 2.5mA (at 2.7V) and 5.1mA (at 5.5V) respectively (applies to resistor values according to Figure 21 and at room temperature).

If the current through T2 is large, the voltage drop through R4 and therefore AADET0_N will be high, indicating an open connection. On the other hand, if the current is small, AADET0_N will be low.

Status Reporting

At startup and on every change of the antenna supervisor configuration the u-blox 5 GPS/GALILEO module will output a NMEA ($GPTXT) or UBX (INF-NOTICE) message with the internal status of the antenna supervisor (disabled, short detection only, enabled).

None, one or several of the strings below are part of this message to inform about the status of the active antenna supervisor circuitry (e.g. "ANTSUPERV= AC SD OD PdoS").

Abbreviation	Description
AC	Antenna Control (e.g. the antenna will be switched on/ off controlled by the GPS receiver)
SD	Short Circuit Detection Enabled
OD	Open Circuit Detection Enabled
PdoS	Power Down on short

Table 9: Active Antenna Supervisor Message on startup (UBX binary protocol)

☞ To activate the antenna supervisor use the UBX-CFG-ANT message. For further information refer to the *u-blox 5 Protocol Specifications [1].*

Similar to the antenna supervisor configuration, the status of the antenna supervisor will be reported in a NMEA ($GPTXT) or UBX (INF-NOTICE) message at start-up and on every change.

Message	Description
ANTSTATUS=DONTKNOW	Active antenna supervisor is not configured and deactivated.
ANTSTATUS=OK	Active antenna connected and powered
ANTSTATUS=SHORT	Antenna short
ANTSTATUS=OPEN	Antenna not connected or antenna defective

Table 10: Active Antenna Supervisor Message on startup (NMEA protocol)

☞ The open circuit supervisor circuitry has a quiescent current of approximately 2mA. This current may be reduced with an advanced circuitry, which fulfils the same function as the u-blox suggested circuitry.

3 Product Handling

☞ All LEA-5 modules are RoHS compliant (lead-free).

3.1 Packaging

LEA-5 modules are delivered as hermetically sealed, reeled tapes in order to enable efficient production, production lot set-up and tear-down.

Figure 22: Reeled u-blox 5 Modules

3.1.1 Reels

LEA-5 modules for GPS and GALILEO are deliverable in quantities of 250pcs on a reel. The dimensions of the reel are shown in *Figure 23*.

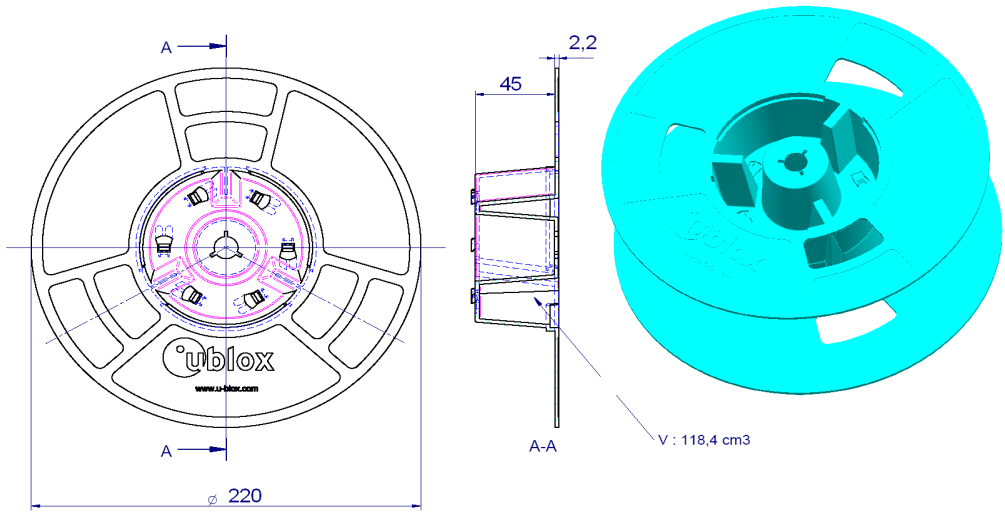


Figure 23: Dimension of reel for 250 pieces (dimensions unless otherwise specified in mm)

3.1.2 Tapes

The dimensions and orientations of the tapes for LEA 5 modules are specified in Figure 24.

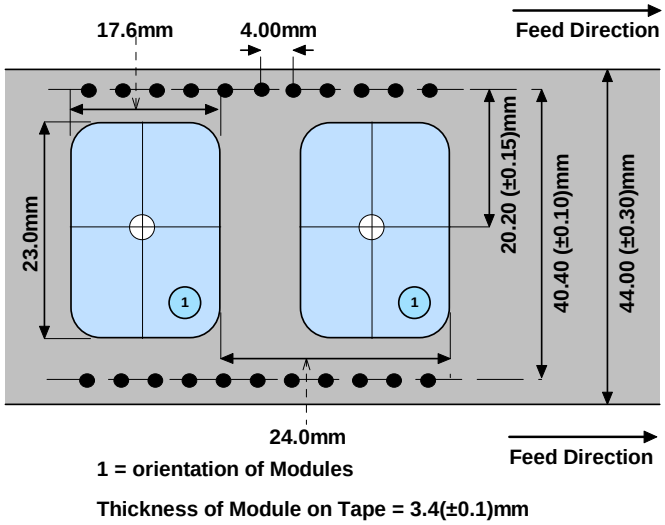


Figure 24: Dimensions and orientation for LEA- 5 modules on tape

3.2 Shipment, Storage and Handling

3.2.1 Handling

u-blox 5 modules are designed and packaged to be processed in an automatic assembly line, and are shipped in Tape-and-Reel.

These components contain highly sensitive electronic circuitry. Handling the LEA-5 modules without proper ESD protection may destroy or damage them permanently.

According to JEDEC ISP, LEA-5 modules are moisture sensitive devices. Appropriate handling instructions and precautions are summarized in *Sections 3.2.2* to *3.2.5.* Read them carefully to prevent permanent damages due to moisture intake.

3.2.2 Shipment

The LEA-5 modules are delivered on Tape-and-Reels in a hermetically sealed package ("dry bag") to prevent moisture intake and protect against electrostatic discharge. For protection from physical damage, the reels are individually packed in cartons.

The dry bag provides a JEDEC compliant MSD label (Moisture Sensitive Devices) describing the handling requirements to prevent humidity intake.

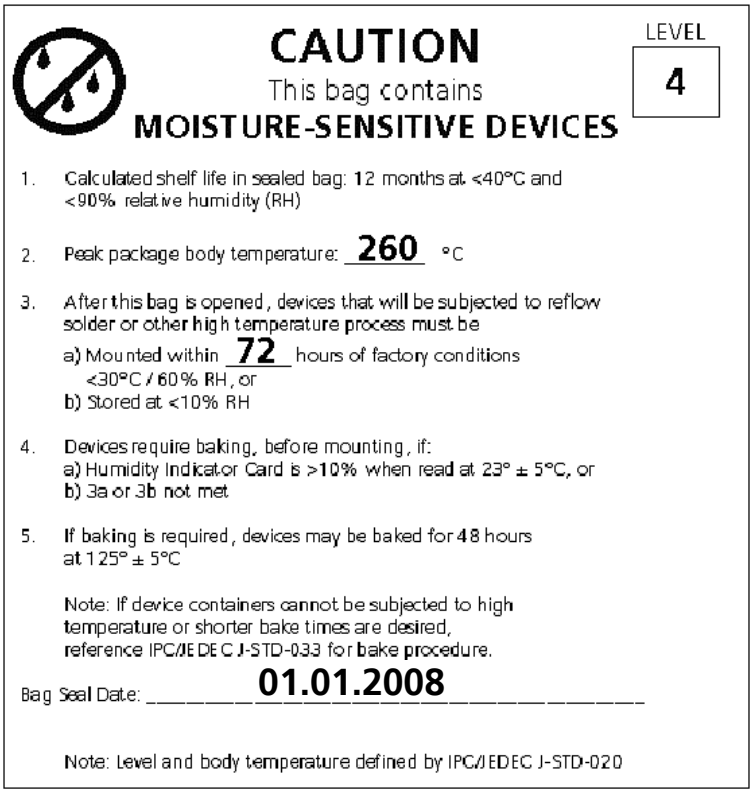


Figure 25: Applicable MSD Label (See *Section 3.1* for baking instructions)

3.2.3 Storage

Shelf life in sealed bag is 12 months at <40°C and <90% relative humidity.

3.2.4 Handling

A humidity indicator card and a desiccant bag to absorb humidity are enclosed in the sealed package. The parts are shipped on tape-and-reel in a hermetically sealed package. If no moisture has been absorbed, the three fields in the humidity indicator card indicate blue color.

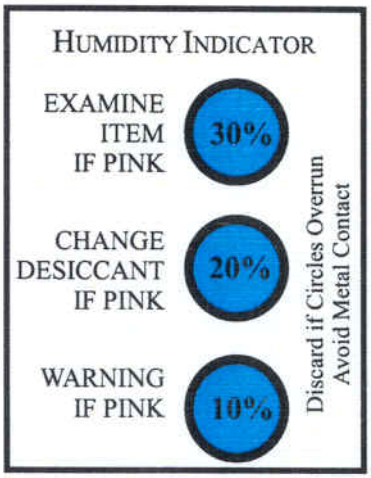


Figure 26: Humidity Indicator Card, good condition

3.2.5 Floor Life

For products with moisture sensitivity level 4, the floor life is 72 hours, or precisely three days. Under factory floor temperature and humidity conditions (<30°C, <60% relative humidity), the parts must be processed and soldered within this specified period of time.

Once the sealed package of the reel is opened and the parts exposed to humidity, they need to be processed within 72 hours (precisely three days) in a reflow soldering process. If this time is exceeded, or the sticker in the sealed package indicates that the goods have been exposed to moisture, the devices need to be pre-baked before the flow solder process. Please refer to *Section 3.3* for instructions on how to pre-bake the components.

3.3 Processing

3.3.1 Moisture Preconditioning

Both encapsulant and substrate materials absorb moisture. JEDEC specification J-STD-020 must be observed to prevent cracking and delamination associated with the "popcorn" effect during solder reflow. The popcorn effect can be described as miniature explosions of evaporating moisture. Baking before processing is required in following cases:

- Humidity indicator card: At least one circular indicator is no longer blue
- Floor life or environmental requirements after opening the seal is opened has been exceeded, e.g. exposure to excessive seasonal humidity.

Recommended baking procedure:

Duration: 48 hours

Temperature: 125°C

Humidity: Below 5%. Desiccant must be placed into the oven to keep humidity low.

Oven: Convection flow oven. Also put desiccant pack into the oven for dehydration.

After work: Put the baked components with desiccant and moisture indicator into a humidity proof bag and use a vacuum hot barrier sealing machine for sealing if not processed within specified floor time. Storage in a nitrogen cabinet or dry box is also a possible approach to prevent moisture intake.

Do not attempt to bake the LEA-5 modules contained in tape and rolled up in reels. If necessary, bake the LEA-5 modules quickly at 125°C for 48 hours, remove them from the belt and place them individually onto the oven tray.

A repeated baking process will reduce the wetting effectiveness of the pad contacts. This applies to all SMT devices.

3.3.2 Soldering Paste

Use of "No Clean" soldering paste is strongly recommended, as it does not require cleaning after the soldering process has taken place. The paste listed in the example below meets these criteria.

Soldering Paste: LFSOLDER TLF-206-93F (Tamura Kaken (UK) Ltd.)

Alloy specification: Sn 95.5/ Ag 3.9/ Cu 0.6 (95.5% Zinc/ 0.6 % Silver/ 0.6% Copper)

Melting Temperature: 216 - 221°C

Stencil Thickness: 150 µm for base boards

The final choice of the soldering paste depends on the approved manufacturing procedures.

The paste-mask geometry for applying soldering paste should meet the recommendations in section 2.8.2.

The quality of the solder joints on the connectors ('half vias') should meet the appropriate IPC specification.

3.3.3 Reflow Soldering

A convection type-soldering oven is strongly recommended over the infrared type radiation oven. Convection heated ovens allow precise control of the temperature and all parts will be heated up evenly, regardless of material properties, thickness of components and surface color.

Consider the "IPC-7530 Guidelines for temperature profiling for mass soldering (reflow and wave) processes, published 2001".

Preheat Phase

Initial heating of component leads and balls. Residual humidity will be dried out. Please note that this preheat phase will not replace prior baking procedures.

- Temperature rise rate: 1 - 4°C/s — If the temperature rise is too rapid in the preheat phase it may cause excessive slumping.
- Time: 60 – 120 seconds — If the preheat is insufficient, rather large solder balls tend to be generated. Conversely, if performed excessively, fine balls and large balls will be generated in clusters.
- End Temperature: 150 - 200°C — If the temperature is too low, non-melting tends to be caused in areas containing large heat capacity.

Heating/ Reflow Phase

The temperature rises above the liquidus temperature of 216 - 221°C. Avoid a sudden rise in temperature as the slump of the paste could become worse.

- Limit time above 220°C liquidus temperature: 20 - 40s
- Peak reflow temperature: 230 - 250°C

Cooling Phase

A controlled cooling avoids negative metallurgical effects (solder becomes more brittle) of the solder and possible mechanical tensions in the products. Controlled cooling helps to achieve bright solder fillets with a good shape and low contact angle.

- Temperature fall rate: max 3°C / s

☞ To avoid falling off, the u-blox 5 GPS/GALILEO module should be placed on the topside of the motherboard during soldering.

The final soldering temperature chosen at the factory depends on additional external factors like choice of soldering paste, size, thickness and properties of the base board, etc. Exceeding the maximum soldering temperature in the recommended soldering profile may permanently damage the module.

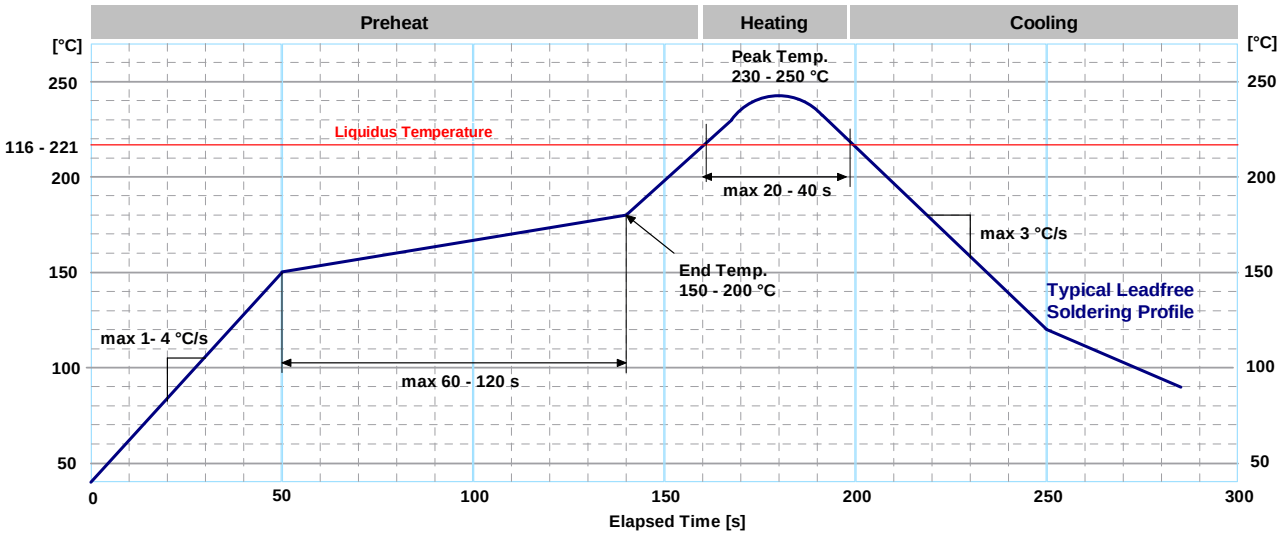


Figure 27: Recommended soldering profile

When soldering leadfree (u-blox 5) modules in a leaded process, check the following temperatures:

- PB- Technology Soaktime: 40-80sec
- Time above Liquidus: 40-90 sec
- Peak temperature: 225-235 °C

LEA-5 modules must not be soldered with a damp heat process.

3.3.4 Optical Inspection

After soldering the LEA-5 module, consider an optical inspection step to check whether:

- The module is properly aligned and centered over the pads
- All pads are properly soldered
- No excess solder has created contacts to neighboring pads, or possibly to pad stacks and vias nearby.

3.3.5 Cleaning

In general, cleaning the populated modules is strongly discouraged. Residues underneath the modules cannot be easily removed with a washing process.

- Cleaning with water will lead to capillary effects where water is absorbed in the gap between the baseboard and the module. The combination of residues of soldering flux and encapsulated water leads to short circuits or resistor-like interconnections between neighboring pads. Water will also damage the sticker and the ink-jet printed text.
- Cleaning with alcohol or other organic solvents can result in soldering flux residues flooding into the two housings, areas that are not accessible for post-wash inspections. The solvent will also damage the sticker and the ink-jet printed text.
- Ultrasonic cleaning will permanently damage the module, in particular the quartz oscillators.

The best approach is to use a "no clean" soldering paste and eliminate the cleaning step after the soldering.

3.3.6 Repeated Reflow Soldering

Only a single reflow soldering process is encouraged for boards with a LEA-5 module populated on it. The reason for this is the risk of the module falling off due to high weight in relation to the adhesive properties of the solder.

3.3.7 Wave Soldering

Base boards with combined through-hole technology (THT) components and surface-mount technology (SMT) devices require wave soldering to solder the THT components. Only a single wave soldering process is encouraged for boards populated with LEA-5 modules.

3.3.8 Hand Soldering

Hand soldering is allowed. Use a soldering iron temperature setting of "7" which is equivalent to 350°C and carry out the hand soldering according to the IPC recommendations / reference documents IPC7711.

Place the module precisely on the pads. Start with a cross-diagonal fixture soldering (e.g. pins 1 and 15), and then continue from left to right.

3.3.9 Rework

The LEA-5 module can be unsoldered from the baseboard using a hot air gun.

Avoid overheating the module.

After the module is removed, clean the pads before placing and hand-soldering a new module.

Never attempt a rework on the module itself, e.g. replacing individual components. Such actions immediately terminate the warranty.

3.3.10 Conformal Coating

Certain applications employ a conformal coating of the PCB using HumiSeal® or other related coating products.

These materials affect the HF properties of the GPS module and it is important to prevent them from flowing into the module.

The RF shields do not provide 100% protection for the module from coating liquids with low viscosity, therefore care is required in applying the coating.

☞ Conformal Coating of the module will void the warranty.

3.3.11 Casting

If casting is required, use viscose or another type of silicon pottant. The OEM is strongly advised to qualify such processes in combination with the LEA-5 module before implementing this in the production.

☞ Casting will void the warranty.

3.3.12 Grounding Metal Covers

Attempts to improve grounding by soldering ground cables, wick or other forms of metal strips directly onto the EMI covers is done at the customer's own risk. The numerous ground pins should be sufficient to provide optimum immunity to interferences and noise.

☞ u-blox makes no warranty for damages to the LEA-5 module caused by soldering metal cables or any other forms of metal strips directly onto the EMI covers.

3.3.13 Use of Ultrasonic Processes

Some components on the LEA-5 module are sensitive to Ultrasonic Waves. Use of any Ultrasonic Processes (cleaning, welding etc.) may cause damage to the GPS Receiver.

☞ u-blox offers no warranty against damages to the LEA-5 module caused by any Ultrasonic Processes.

4 Product Testing

4.1 u-blox In-Series Production Test

u-blox focuses on high quality for its products. To achieve a high standard it's our philosophy to supply fully tested units. Therefore at the end of the production process, every unit is tested. Defective units are analyzed in detail to improve the production quality.

This is achieved with automatic test equipment, which delivers a detailed test report for each unit. The following measurements are done:

- Digital self-test (Software Download, verification of FLASH firmware, etc.)
- Measurement of voltages and currents
- Measurement of RF characteristics (e.g. C/No)

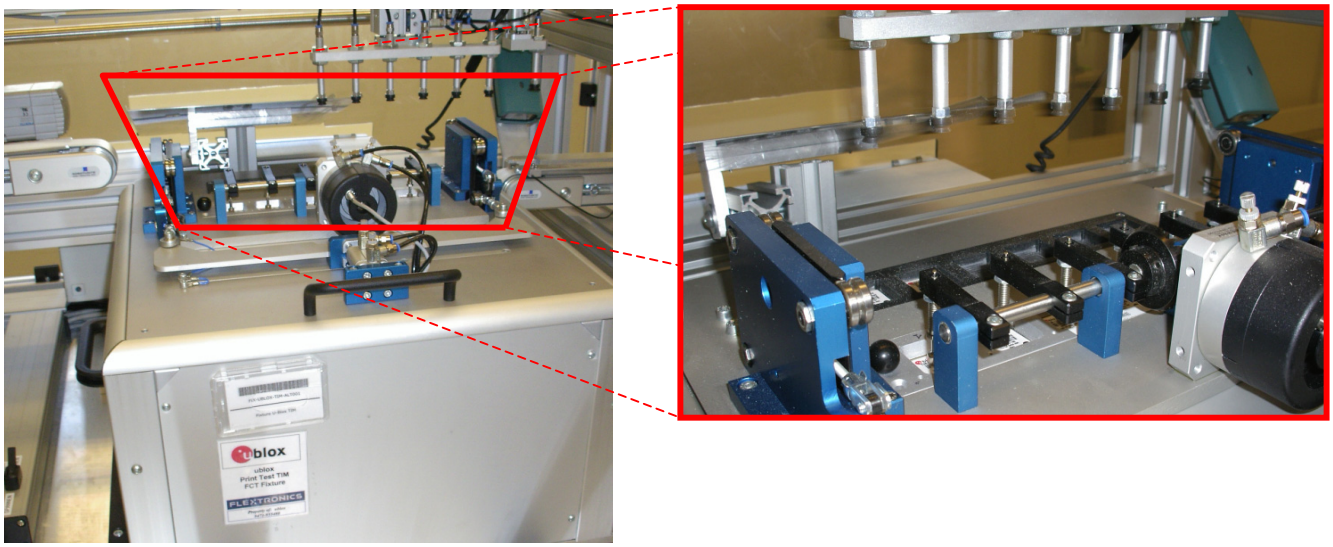


Figure 28: Automatic Test Equipment for Module Tests

4.2 Test Parameters for OEM Manufacturer

Because of the testing done by u-blox (with 100% coverage), it is obvious that an OEM manufacturer doesn't need to repeat firmware tests or measurements of the GPS parameters/characteristics (e.g. TTFF) in their production test.

An OEM Manufacturer should focus on

- Overall sensitivity of the device (including antenna, if applicable)
- Communication to a host controller

4.3 System Sensitivity Test

The best way to test the sensitivity of a GPS device is with the use of a 1-channel GPS simulator. It assures reliable and constant signals at every measurement.

Figure 29: 1-channel GPS simulator

u-blox recommends the following Single-Channel GPS Simulator:

- Spirent GSS6100
  Spirent Communications Positioning Technology
  (previously GSS Global Simulation Systems) www.positioningtechnology.co.uk

4.3.1 Guidelines for Sensitivity Tests

1. Connect a 1-channel GPS simulator to the OEM product
2. Choose the power level in a way that the "Golden Device" would report a C/No ratio of 38-40 dBHz
3. Power up the DUT (Device Under Test) and allow enough time for the acquisition
4. Read the C/No value from the NMEA GSV or the UBX-NAV-SVINFO message (e.g. with u-center)
5. Compare the results to a "Golden Device" or a u-blox 5 Evaluation Kit.

4.3.2 'Go/No go' tests for integrated devices

The best test is to bring the device to an outdoor position **with excellent sky view** (HDOP < 3.0). Let the receiver acquire satellites and compare the signal strength with a "Golden Device".

☞ As the electro-magnetic field of a redistribution antenna is not homogenous, indoor tests are in most cases not reliable. These kind of tests may be useful as a 'go/no go' test but not for sensitivity measurements.

Appendix

A Migration to u-blox 5 Receivers

Migrating ANTARIS®4 to a u-blox 5 receiver module is a fairly straightforward procedure. Nevertheless there are some points to be considered during the migration.

☞ Not all of the functionalities available with ANTARIS®4 are supported by u-blox 5. These include:

- FixNow Mode
- Low Power Modes
- RTCM
- UTM

A.1 Migration from LEA-4H / LEA-4P to LEA-5H

The pin-outs of LEA-4 and LEA-5H differ slightly. Table 11 and Table 12 compare the modules and highlight the differences to be considered.

Pin	LEA-4H/LEA-4P/LEA-4T		LEA-5H/LEA-5T		Remarks for Migration
	Pin Name	Typical Assignment	Pin Name	Typical Assignment	
1	**Reserved**	VDDIO level I/O; not connected	**SDA2**	NC	
2	**Reserved**	VDDIO level I/O; not connected	**SCL2**	NC	
3	**TXD1**	VDDIO level I/O	**TxD1**	Output	
4	**RXD1**	VDDIO level I/O	**RxD1**	Input	Leave open if not used.
5	**VDDIO**	1.65 – 3.60V	**NC**	Connect to VCC	Can be left open, but connection to VCC is recommended for compatibility reason (e.g LEA-5Q). With LEA-5H the I/O voltage is always VCC.
6	**VCC**	2.70 – 3.30V	**VCC**	2.70 – 3.60V	Extended power supply range, higher peak supply current.
7	**GND**	GND	**GND**	GND	No difference
8	**VDD18OUT**	NC	**VCC_OUT**	NC	Internally connected to VCC, if you have circuitry connected to this pin, check if it withstands the VCC voltage.
9	**Reserved**	NC	**Reserved**	NC	
10	**RESET_N**	1.8V	**RESET_N**	NC	Input only, do not drive high. Internal pull up to VCC.
11	**V_BAT**	1.50 – 3.6V	**V_BCKP**	1.40 – 4.8V	Wider voltage range but needs more current. Check your backup supply, regarding the higher consumption.
12	**BOOT_INT**	NC	**Reserved**	NC	do not drive low.
13	**GND**	GND	**GND**	GND	No difference
14	**GND**	GND	**GND**	GND	No difference
15	**GND**	GND	**GND**	GND	No difference
16	**RF_IN**	RF_IN	**RF_IN**	RF_IN	No difference
17	**GND**	GND	**GND**	GND	No difference
18	**VCC_RF**	VCC - 0.1V	**VCC_RF**	VCC - 0.1V	No difference
19	**V_ANT**	3.0V –5.0V	**V_ANT**	2.7V -5.5V	No difference
20	**AADET_N**	NC	**AADET0_N**	NC	
21	**EXTINT1**	NC	**NC**	NC	
22	**Reserved**	NC	**NC**	NC	
23	**Reserved**	NC	**NC**	NC	
24	**VDDUSB**	Connected to GND or VDD_USB	**VDDUSB**	Connected to GND or VDD_USB	Do not leave open. (VDD_USB is 3.3V regulated power supply from VBUS.)
25	**USB_DM**	NC	**USB_DM**	NC	No difference
26	**USB_DP**	NC	**USB_DP**	NC	No difference
27	**EXTINT0**	NC	**EXTINT0**	NC	
28	**TIMEPULSE**	VDDIO level I/O	**TIMEPULSE**	Output	

: Pins to be checked carefully; NC: Not connected

Table 11: Pin-out comparison LEA-4H/LEA-4P/LEA-4T vs. LEA-5H/LEA-5T

Pin	LEA-4A/LEA-4S		LEA-5A/LEA-5S		Remarks for Migration
	Pin Name	Typical Assignment	Pin Name	Typical Assignment	
1	**TxD2**	3.0V out	**SDA2**	NC	
2	**RxD2**	1.8 - 5.0V	**SCL2**	NC	
3	**TxD1**	3.0V out	**TxD1**	Output	
4	**RxD1**	1.8 - 5.0V in	**RxD1**	Input	Leave open if not used.
5	**VDDIO**	VCC	**NC**	Connect to VCC	Can be left open, but connection to VCC is recommended for compatibility reason (e.g LEA-5Q).
6	**VCC**	2.70 – 3.30V	**VCC**	2.70 – 3.60V	Extended power supply range, higher peak supply current.
7	**GND**	GND	**GND**	GND	No difference
8	**VDD18OUT**	1.8V out	**VCC_OUT**	NC	Internally connected to VCC, if you have circuitry connected to this pin, check if it withstands the VCC voltage.
9	**GPSMODE6**	NC (GND or VDD18OUT)	**CFG_COM1**	NC	
10	**RESET_N**	*ACTIVE LOW*	**RESET_N**	NC	Input only, do not drive high. Internal pull up to VCC.
11	**V_BAT**	1.50 – 3.6V	**V_BCKP**	1.30 – 4.8V	Wider voltage range but needs more current. Check your backup supply, regarding the higher consumption.
12	**BOOT_INT**	NC	**Reserved**	NC	do not drive low.
13	**GND**	GND	**GND**	GND	No difference
14	**GND**	GND	**GND**	GND	No difference
15	**GND**	GND	**GND**	GND	No difference
16	**RF_IN**	RF_IN	**RF_IN**	RF_IN	No difference
17	**GND**	GND	**GND**	GND	No difference
18	**VCC_RF**	VCC - 0.1V	**VCC_RF**	VCC - 0.1V	No difference
19	**V_ANT**	3.0V - 5.0V	**V_ANT**	3.0V -5.0V	No difference
20	**AADET_N**	NC (1.8 to 5.0V)	**AADET0_N**	NC	
21	**GPSMODE5**	NC (GND or VDD18OUT)	**NC**	NC	
22	**GPSMODE2 GPSMODE2 3**	NC (GND or VDD18OUT)	**NC**	NC	
23	**GPSMODE7**	NC (1.8 to 5.0V)	**NC**	NC	
24	**VDDUSB**	3.0 –3.6V/ GND	**VDDUSB**	Connected to GND or VDD_USB	Do not leave open. (VDD_USB is 3.3V regulated power supply from VBUS.)
25	**USB_DM**	VDDUSB I/O	**USB_DM**[7]	NC	No difference
26	**USB_DP**	VDDUSB I/O	**USB_DP**Error! Bookmark not defined.	NC	No difference
27	**EXTINT0**	NC (1.8 to 5.0V)	**EXTINT0**	NC	
28	**TIMEPULSE**	VDDIO out	**TIMEPULSE**	Output	

: Pins to be checked carefully; NC: Not connected

Table 12: Pin-out comparison LEA-4H/LEA-4P/LEA-4T vs. LEA-5H/LEA-5T

[7] Planned availability Q1/09 for LEA-5S and LEA-5A

B Reference Design

B.1 LEA-5 Smart Antenna

The following design supports all LEA-5 modules on one PCB and features one serial port as well as a USB connection. If USB is not needed some components can be spared.

☞ For this design u-blox provides a complete Smart Antenna Demo Design including Schematic, Gerber Files, PCB blueprint and recommendations. Contact u-blox support for further information. Conditions apply.

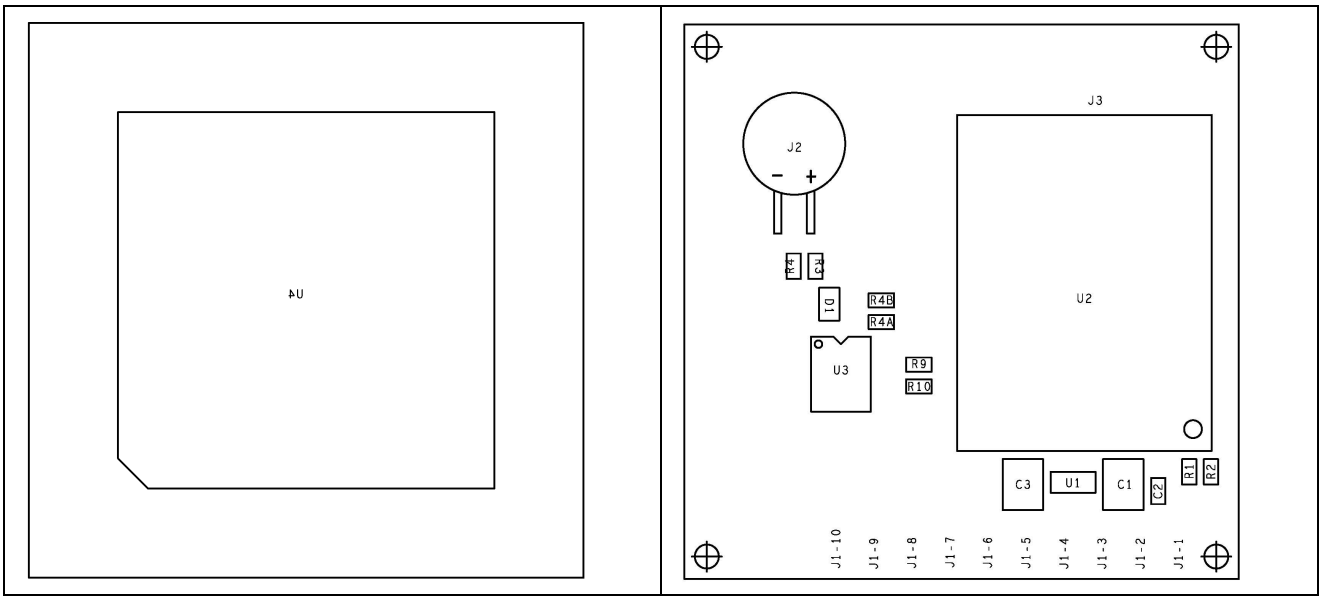


Figure 30: LEA-Smart Antenna (top view/ bottom view)

B.1.1 Schematic

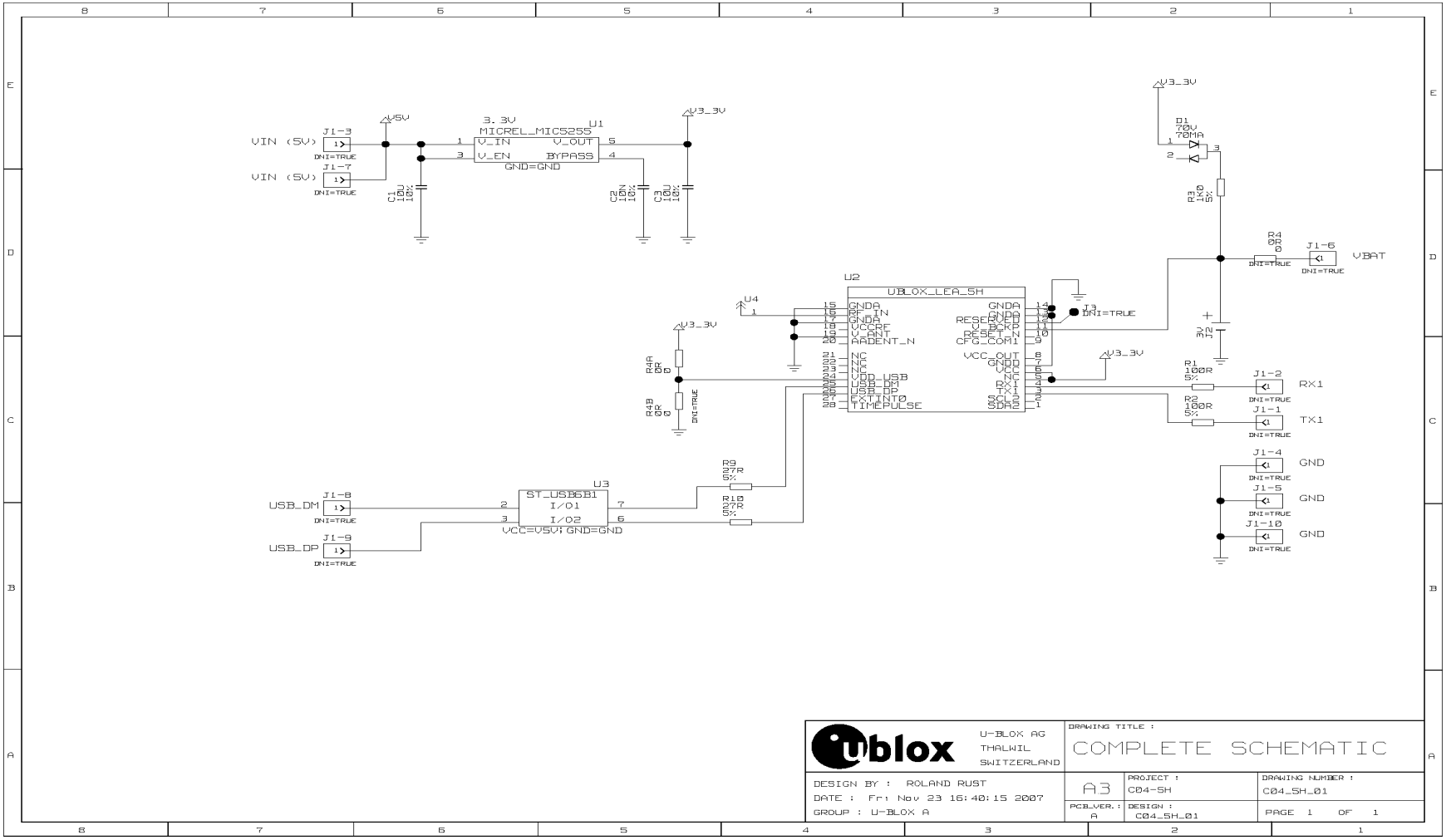


Figure 31: LEA Smart Antenna Schematic

B.1.2 Bill of Material

	Part description	Remarks
C1, C3	CER X5R 1210 10µ 10% 10V ROHS	
C2	CER X7R 0603 10n 10% 25V ROHS	
D1	SCHOTTKY DIODE INFINEON BAS70-04W 70V 70MA ROHS	Only required if optional battery J2 is used.
J2	BATTERY PANASONIC 3V 5MVA ML621S ROHS	Optional. If not used, connect pin J1-6 to battery on motherboard or to GND.
R1 R2	RES THICK FILM CHIP 0603 100R 5% 0.1W ROHS	
R10 R9	RES THICK FILM CHIP 0603 27R 5% 0.1W ROHS	Do not fit if USB is not used.
R3	RES THICK FILM CHIP 0603 1K0 5% 0.1W ROHS	Only required if optional battery J2 is used.
R4	RES THICK FILM CHIO 0603 0R 0.1W ROHS	Only required if optional battery J2 is not used.
R4A	RES THICK FILM CHIP 0603 0R 0.1W ROHS	Fit only if USB is used.
R4B	RES THICK FILM CHIO 0603 0R 0.1W ROHS	Fit only if USB is used.
U1	LOW DROPOUT REGULATOR MICREL MIC5255 3.3V 150MA SOT23 ROHS	
U2	GPS RECEIVER U-BLOX LEA-5H-0-000 ROHS	
U3	USB DATA LINE PROTECTION ST USB6B1 SO8 ROHS	Do not fit if USB is not used
U4	CERAMIC PATCH ANTENNA TH 25mm x 25mm FO=1575 ROHS	e.g. INPAQ PA1575MZ50I4G-13-13/1589 (see also section Appendix C for more information)

Table 13: Bill of Material

☞ Depending on the required interface (USB or UART), several parts don't have to be fit. The same applies to the backup battery if an external backup supply is available. Refer to Table 13 for the feasible options.

B.1.3 Layout

The layout is designed for a 2-layer **1mm FR4 PCB board**.

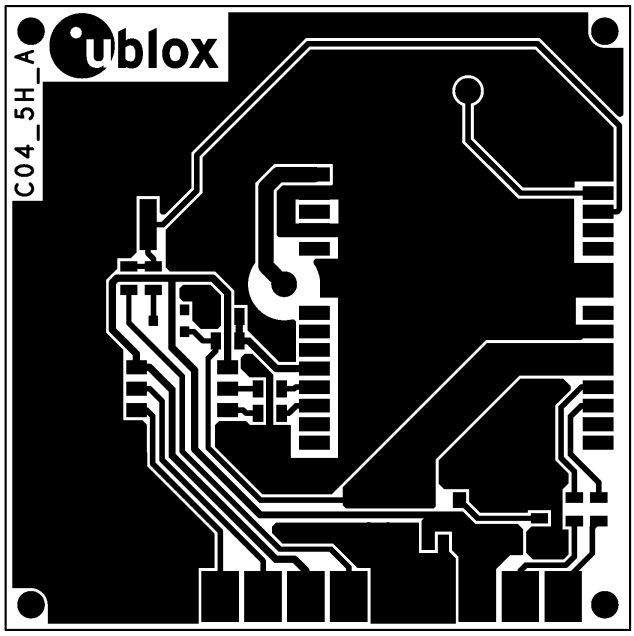


Figure 32: Top Layer

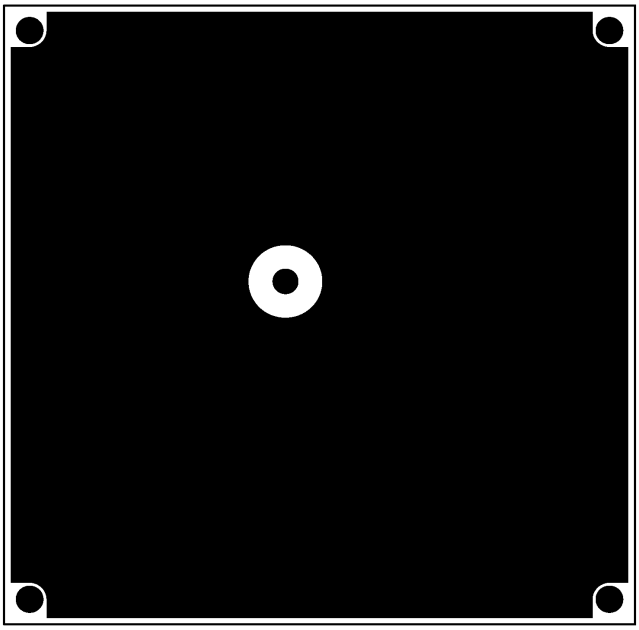


Figure 33: Bottom Layer

C Antennas

Even the best receiver cannot bring back what has been lost at the antenna. The importance of the attention paid to this part of a GPS/GALILEO system cannot be stated highly enough.

C.1 Selecting the right Antenna

Several different antenna designs are available on the GPS/GALILEO applications market. The GPS/GALILEO L1 signal is right-hand circular polarized (RHCP). This results in a style of antenna that is different from the well-known whip antennas used for linear polarized signals. The foremost antennas for GPS/GALILEO application designs are the patch antennas as shown in Figure 34.

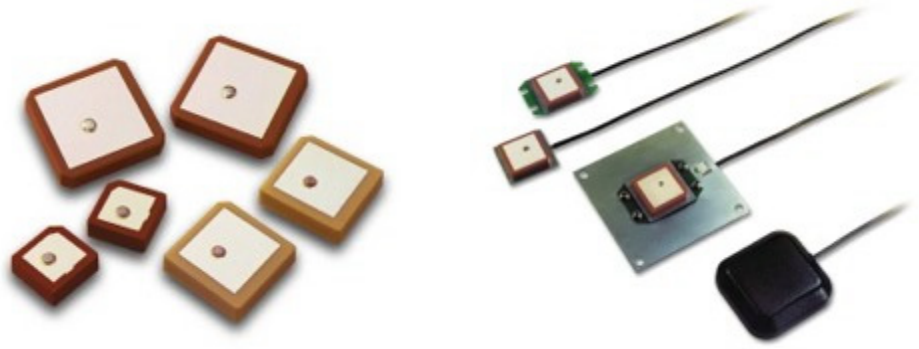


Figure 34: Patch Antennas, EMTAC Technology Corp.

Another style is the quadrifilar helix antenna shown in Figure 35. The actual geometric size of both antenna designs depends on the dielectric that fills the space between the active parts of the antenna. If the antenna is only loaded with air it will be comparatively large, high dielectric constant ceramics result in a much smaller form factor. The smaller the dimensions of the antenna, the more performance critical tight manufacturing tolerances become. Furthermore, a smaller antenna will present a smaller aperture to collect the signal energy from sky resulting in a lower overall gain of the antenna. This is the result of pure physics and there is no "magic" to get around this problem. Amplifying the signal after the antenna will not improve the signal to noise ratio.

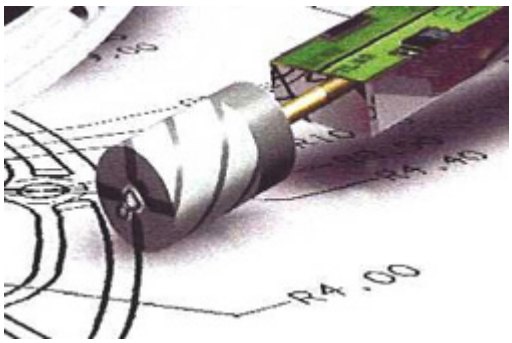


Figure 35: Quadrifilar Helix Antenna, Sarantel, Ltd.

In contrast to helix antennas, patch antennas require a ground plane for operation. Helix antennas can be designed for use with or without a ground plane.

For precision applications such as surveying or timing, some very high caliber antenna systems exist. Common to these designs are large size, high power consumption and high cost. These designs are highly optimized to suppress multi-path signals reflected from the ground (choke ring antennas, multi-path limiting antennas, MLA).

Another area of optimization is accurate determination of the phase center of the antenna. For precision GPS/GALILEO applications with position resolution in the millimeter range it is important that signals from satellites at all elevations virtually meet at exactly the same point inside the antenna. For these types of applications receivers with multiple antenna inputs are often required.

At the low end of the spectrum of possible antenna solutions - if the user is willing to accept significant signal losses - a simple linear polarized whip or strip antenna will work. Compared to a circular polarized antenna, a minimum of 3 dB of signal to noise ratio will be lost.

C.2 Active and Passive Antennas

Passive antennas contain only the radiating element, e.g. the ceramic patch or the helix structure. Sometimes they also contain a passive matching network to match the electrical connection to 50 Ohms impedance.

Active antennas have an integrated low-noise amplifier. This is beneficial in two respects. Firstly, the losses of the cable no longer affect the overall noise figure of the GPS/GALILEO receiver system. Secondly, the receiver noise figure can be much higher without sacrificing performance. Therefore, some receivers will only work with active antennas. Active antennas require a power supply that contributes to total GPS/GALILEO system power consumption, typically in the region of 5 to 20 mA. Usually, the supply voltage is fed to the antenna through the coaxial RF cable. Inside the antenna, the DC component on the inner conductor will be separated from the RF signal and routed to the supply pin of the LNA.

The use of an active antenna is always advisable if the RF-cable length between receiver and antenna exceeds approximately 10 cm. Care should be taken that the gain of the LNA inside the antenna does not lead to an overload condition at the receiver. For receivers that also work with passive antennas, an antenna LNA gain of 15 dB is usually sufficient, even for cable lengths up to 5 m. There's no need for the antenna LNA gain to exceed 26 dB for use with u-blox receivers. With shorter cables and a gain above 25 dB, an overload condition might occur on some receivers.

When comparing gain measures of active and passive antennas one has to keep in mind that the gain of an active antenna is composed of two components, the antenna gain of the passive radiator, given in dBic, and the LNA power gain given in dB. A low antenna gain cannot be compensated by high LNA gain. If a manufacturer provides one total gain figure, this is not sufficient to judge the quality of the antenna. One would need information on antenna gain (in dBic), amplifier gain, and amplifier noise figure.

C.3 Patch Antennas

Patch antennas are ideal for an application where the antenna sits on a flat surface, e.g. the roof of a car. Patch antennas can demonstrate a very high gain, especially if they are mounted on top of a large ground plane. Ceramic patch antennas are very popular because of their small size, typically measuring 25 x 25 mm^2 down to 12 x 12 mm^2. Very cheap construction techniques might use ordinary circuit board material like FR-4 or even air as a dielectric, but this will result in a much larger size, typically in the order of 10 x 10 cm^2. Figure 36 shows a typical example of the radiation pattern of a 16 x 16 mm^2 ceramic patch antenna. This measurement only shows the upper sphere of the radiation pattern. Depending on ground plane size there will also be a prominent back lobe present.

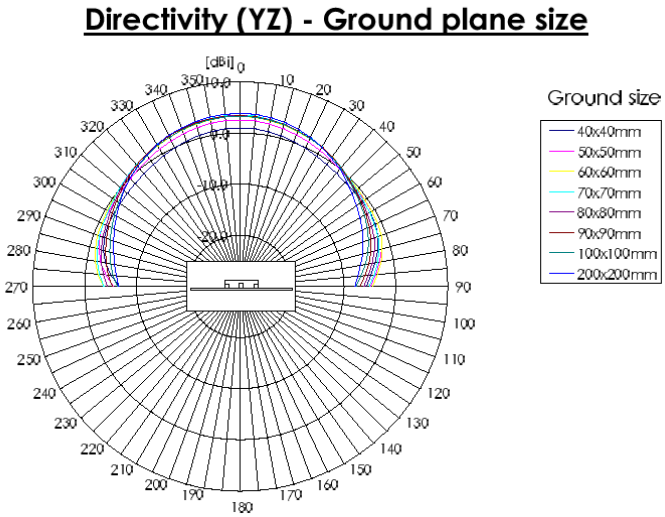


Figure 36: Typical Radiation Pattern of a Patch Antenna, MuRata, Inc.

For the specific example shown in Figure 37 one can easily see that the so-called axial ratio, the relation of major to minor axis of the elliptical polarization has a minimum at the 50 mm^2 square ground plane. At this point, the polarization of the antenna is closest to an ideal circular polarization (axial ratio = 0 dB). At a 100 mm^2 square ground plane size this particular patch shows an axial ratio in the order of 10 dB, which is closer to linear polarization than to circular and will result in respective losses. This effect can also be seen in the left graph of the figure, where gain no longer increases with increasing ground plane size. In conclusion, the correct dimensions for the size of the ground plane can serve as a useful compromise between maximum gain and reasonable polarization loss.

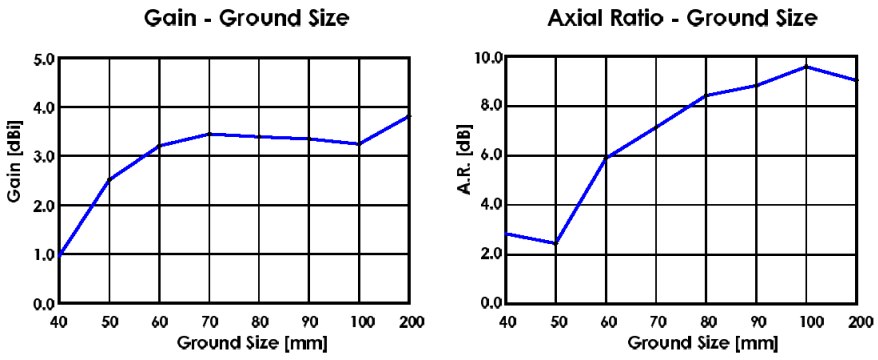


Figure 37: Typical Gain and Axial Ratio of a Patch antenna with respect to ground plane size, MuRata, Inc.

A good allowance for ground plane size is typically in the area of 50 to 70 mm^2. This number is largely independent of the size of the patch itself (when considering ceramic patches). Patch antennas with small ground planes will also have a certain back-lobe in their radiation pattern, making them susceptible to radiation coming from the backside of the antenna, e.g. multi-path signals reflected off the ground. The larger the size of the ground plane, the less severe this effect becomes.

Smaller sized patches will usually reach their maximum gain with a slightly smaller ground plane compared to a larger size patch. However, the maximum gain of a small sized patch with optimum ground plane may still be much lower than the gain of a large size patch on a less than optimal ground plane.

It is not only gain and axial ratio of the patch antenna that is affected by the size of the ground plane but also the matching of the antenna to the 50 Ohms impedance of the receiver. See *Appendix C.6* for more information on matching.

C.4 Helix Antennas

Helix antennas can be designed for use with or without ground plane. For example, the radiating elements on board the GPS and GALILEO satellites have a ground plane. Using an array of helix antennas, the GPS and GALILEO satellites can control the direction of the emitted beam. If a helix antenna is designed without ground plane it can be tuned such to show a more omni directional radiation pattern as shown in Figure 38.

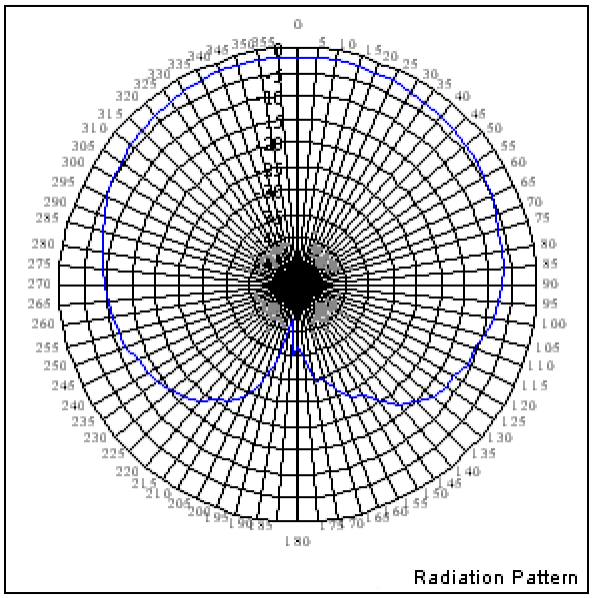


Figure 38: Radiation pattern of helix antenna without ground plane, Sarantel, Ltd.

Although we can determine an axial ratio close to 9 dB between zero degree and 90 degrees elevation, which compares to the patch antenna, the back lobe of the helix generally degrades much smoother and does not show any sensitivity at the –180 degree direction. In contrast, the back lobe of a patch antenna depends very much on size and shape of the ground plane. As with patch antennas, filling the antenna with a material with a high dielectric constant can reduce the size of helix antennas. Sizes in the order of 18 mm length and 10 mm diameter are being offered on the market. Again, antenna gain will decrease with decreased size.

C.5 Helix or Patch, which selection is best?

For practical applications the possibilities of integrating a certain style of antenna into the actual device is of primary concern. Some designs naturally prefer the patch type of antenna, e.g. for rooftop applications. Others prefer the pole like style of the helix antenna, which is quite similar to the style of antennas used in mobile phones. Furthermore, it is important that the antenna's main lobe points to the sky in order to receive as many satellites as possible with maximum gain. If the application is a hand held device, the antenna should be designed in such a way that natural user operation results in optimum antenna orientation. The helix antenna seems to be more appropriate in this respect.

However, one has to keep in mind that comparable antenna gain requires comparable size of the antenna aperture, which will lead to a larger volume filled by a helix antenna in comparison to a patch antenna. Helix antennas with a "reasonable" size will therefore typically show a lower sensitivity compared to a "reasonably" sized patch antenna.

A helix antenna might result in a "more satellites on the screen" situation in difficult signal environments when directly compared with a patch antenna. This is due to the fact that the helix will more easily pick up signals through its omni directional radiation pattern. However, the practical use of these signals is very limited because of the uncertain path of the reflected signals. Therefore, the receivers can see more satellites but the navigation solution will be degraded because of distorted range measurements in a multi-path environment.

If possible test the actual performance of different antenna types in a real life environment before starting the mechanical design of the GPS/GALILEO enabled product.

C.6 Antenna Matching

All common GPS/GALILEO antennas are designed for a 50 Ohms electrical load. Therefore, one should select a 50 Ohms cable to connect the antenna to the receiver. However, there are several circumstances under which the matching impedance of the antenna might shift considerably. Expressed in other words, this means that the antenna no longer presents a 50 Ohms source impedance. Typically what happens is that the center frequency of the antenna is shifted away from GPS/GALILEO frequency - usually towards lower frequencies – by some external influence. The reasons for this effect are primarily disturbances in the near field of the antenna. This can either be a ground plane, that does not have the size for which the antenna was designed , or it can be an enclosure with a different dielectric constant than air.

In order to analyze effects like this one would normally employ electrical field simulations, which will result in exact representation of the electric fields in the near field of the antenna. Furthermore, these distortions of the near field will also show their effect in the far field, changing the radiation pattern of the antenna. Unfortunately, there is no simple formula to calculate the frequency shift of a given antenna in any specified environment. So one must do either extensive simulation or experimental work. Usually, antenna manufacturers offer a selection of pre-tuned antennas, so the user can test and select the version that best fits the given environment. However, testing equipment such as a scalar network analyzer is needed to verify the matching.

Again, it must be pointed out that the smaller the size of the antenna, the more sensitive it will be to distortions in the near field. Also the antenna bandwidth will decrease with decreasing antenna size, making it harder to achieve optimum tuning.

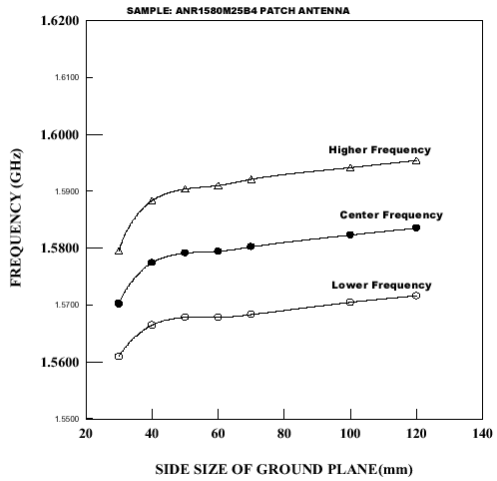


Figure 39: Dependency of center frequency on ground plane dimension for a 25 x 25 mm² patch, EMTAC

A LNA placed very close to the antenna can help to relieve the matching requirements. If the interconnect length between antenna and LNA is much shorter than the wavelength (9.5 cm on FR-4), the matching losses become less important. Under these conditions the matching of the input to the LNA becomes more important. Within a reasonable mismatch range, integrated LNAs can show a gain decrease in the order of a few dBs versus an increase of noise figure in the order of several tenths of a dB. If your application requires a very small antenna, a LNA can help to match the hard to control impedance of the antenna to a 50 Ohms cable. This effect is indeed beneficial if the antenna cable between the antenna and the receiver is only short. In this case, there's no need

for the gain of the LNA to exceed 10-15 dB. In this environment the sole purpose of the LNA is to provide impedance matching and not signal amplification.

C.7 Antenna Placement

The location where the antenna is mounted is crucial for optimal performance of the GPS/GALILEO receiver.

When using patch antennas, the antenna plane should be parallel to the geographic horizon. The antenna must have full view of the sky ensuring a direct line-of-sight with as many visible satellites as possible.

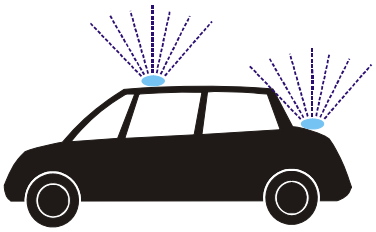
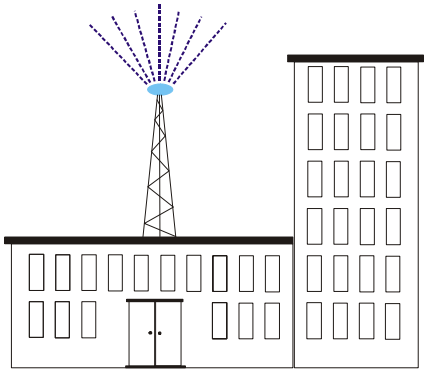
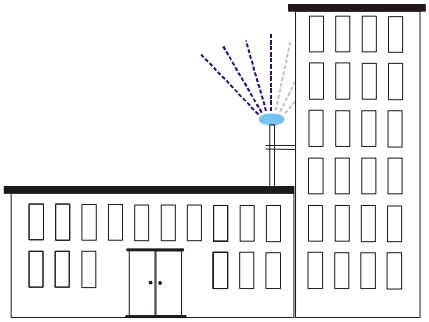
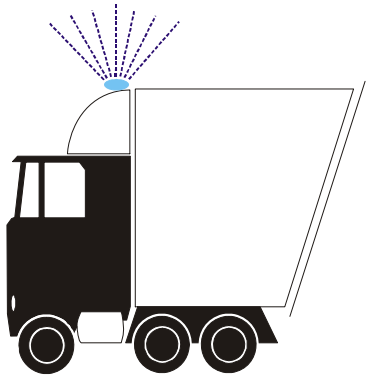
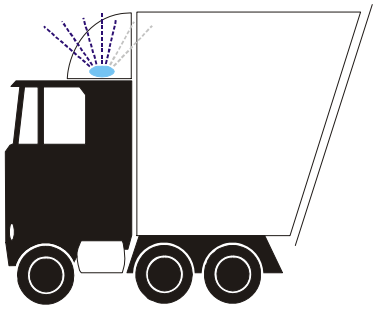
1st Choice Placement	2nd Choice Placement
Recommended Antenna positions	Performance may be degraded! If recommended placements are not available, these may also viable.
	 ☞ **Note: Window and roof reduce GPS signal and obstruct sky view**[8]
	 ☞ **Note: There may be multipath signals and an obstructed sky view**
	 ☞ **Note: Fiberglass airfoil attenuates the GPS/GALILEO signal**

Table 14: Optimal antenna placement

[8] Some cars have a metallic coating on the windscreens. GPS/GALILEO reception may not be possible in such a car without the use of SuperSense® Technology. There is usually a small section, typically behind the rear view mirror, reserved for mobile phone and GPS/GALILEO antennas.

D Interference Issues

A typical GPS/GALILEO receiver has a very low dynamic range. This is because the antenna should only detect thermal noise in the GPS/GALILEO frequency band, given that the peak power of the GPS/GALILEO signal is 15 dB below the thermal noise floor. This thermal noise floor is usually very constant over time. Most receiver architectures use an automatic gain control (AGC) circuitry to automatically adjust to the input levels presented by different antenna and pre-amplifier combinations. The control range of these AGC's can be as large as 50 dB. However, the dynamic range for a jamming signal exceeding the thermal noise floor is typically only 6 to 12dB, due to the one or two bit quantization schemes commonly used in GPS/GALILEO receivers. If there are jamming signals present at the antenna and the levels of these signals exceed the thermal noise power, the AGC will regulate the jamming signal, suppressing the GPS/GALILEO signal buried in thermal noise even further. Depending on the filter characteristics of the antenna and the front end of the GPS/GALILEO receiver, the sensitivity to such in-band jamming signals decreases more or less rapidly if the frequency of the jamming signal moves away from GPS/GALILEO signal frequency. We can conclude that a jamming signal exceeding thermal noise floor within a reasonable bandwidth (e.g. 100 MHz) around GPS/GALILEO signal frequency will degrade the performance significantly.

Even out-of-band signals can affect GPS/GALILEO receiver performance. If these jamming signals are strong enough that even antenna and front-end filter attenuation are not sufficient, the AGC will still regulate the jamming signal. Moreover, very high jamming signal levels can result in non-linear effects in the pre-amplifier stages of the receiver, resulting in desensitizing of the whole receiver. One such particularly difficult scenario is the transmitting antenna of a DCS handset (max. 30 dBm at 1710 MHz) in close proximity to the GPS/GALILEO antenna. When integrating GPS/GALILEO with other RF transmitters special care is necessary.

If the particular application requires integration of the antenna with other digital systems, one should make sure that jamming signal levels are kept to an absolute minimum. Even harmonics of a CPU clock can reach as high as 1.5 GHz and still exceed thermal noise floor.

On the receiver side there's not much that can be done to improve the situation without significant effort. Of course, high price military receivers have integrated counter-measures against intentional jamming. But the methods employed are out of the scope of this document and might even conflict with export restrictions for dual-use goods.

The recommendations and concepts in this section are completely dependent on the specific applications. In situations where an active antenna is used in a remote position, e.g. >1 m away from other electronics, interference should not be an issue.

☞ If antenna and electronics are to be tightly integrated, the following sections should be read very carefully.

D.1 Sources of Noise

Basically two sources are responsible for most of the interference with GPS receivers:

1. Strong RF transmitters close to GPS frequency, e.g. DCS at 1710 MHz or radars at 1300 MHz.
2. Harmonics of the clock frequency emitted from digital circuitry.

The first problem can be very difficult to solve, but if GPS/GALILEO and RF transmitter are to be integrated close to each other, there's a good chance that there is an engineer at hand who knows the specifications of the RF transmitter. In most cases, counter measures such as filters will be required for the transmitter to limit disruptive emissions below the noise floor near the GPS/GALILEO frequency.

Even if the transmitter is quiet in the GPS/GALILEO band, a very strong emission close to it can cause saturation in the front-end of the receiver. Typically, the receiver's front-end stage will reach its compression point, which will in turn increase the overall noise figure of the receiver. In that case, only special filtering between the GPS/GALILEO antenna and receiver input will help to reduce signal levels to the level of linear operation at the front-end.

The second problem is more common but also regularly proves to be hard to solve. Here, the emitting source is not well specified and the emission can be of broadband nature, making specific countermeasures very difficult. Moreover, the GPS/GALILEO band is far beyond the 1 GHz limit that applies to almost all EMC regulations. So, even if a device is compliant with respect to EMC regulations it might severely disturb a GPS receiver.

If the GPS/GALILEO antenna is to be placed very close to some other electronics, e.g. the GPS/GALILEO receiver itself or a PDA-like appliance, the EMC issue must be taken very seriously right from the concept phase of the design. It is one of the most demanding tasks in electrical engineering to design a system that is essentially free of measurable emissions in a given frequency band.

D.2 Eliminating Digital Noise Sources

Digital noise is caused by short rise-times of digital signals. Data and address buses with rise-times in the nanosecond range will emit harmonics up to several GHz. The following sections contain some general hints on how to decrease the level of noise emitted from digital circuit board that are potentially in close proximity to the GPS receiver or the antenna.

D.2.1 Power and Ground Planes

Use solid planes for power and ground interconnect. This will typically result in a PCB with at least four layers but will also result in a much lower radiation. Solid ground planes ensure that there is a defined return path for the signals routed on the signal layer. This will reduce the "antenna" area of the radiating loop. Planes should be solid in a sense that there are no slots or large holes inside the plane.

The outer extent of the power plane should be within the extent of the ground plane. This avoids that the edges of the two planes form a slot antenna at the board edges. It's a good idea to have a ground frame on the circumference of every layer that is connected to the ground plane with as many vias as possible. If necessary, a shield can then be easily mounted on top of this frame (see Figure 40). Furthermore, free space on the outermost Layers can be filled with ground shapes connected to the ground plane to shield radiation from internal layers.

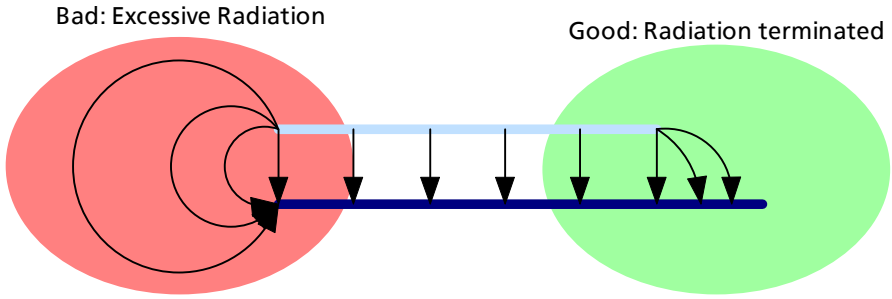


Figure 40: Signal and power plane extends should lie within ground plane extends

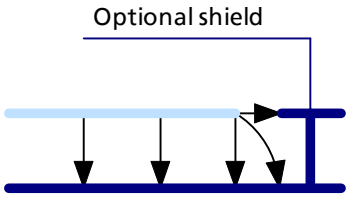


Figure 41: Further improvement of reduction of power plane radiation

D.2.2 High Speed Signal Lines

Keep high-speed lines as short as possible. This will reduce the area of the noise-emitting antenna, i.e. the conductor traces. Furthermore, the use of line drivers with controlled signal rise-time is suggested whenever driving large bus systems. Alternatively, high-speed signal lines can be terminated with resistors or even active terminations to reduce high frequency radiation originating from overshoot and ringing on these lines.

If dielectric layers are thick compared to the line width, route ground traces between the signal lines to increase shielding. This is especially important if only two layer boards are used (see Figure 42).

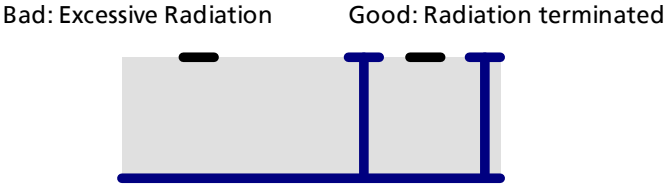


Figure 42: Terminating radiation of signal lines

D.2.3 Decoupling Capacitors

Use a sufficient number of decoupling capacitors in parallel between power and ground nets. Small size, small capacitance types reduce high-frequency emissions. Large size, high capacitance types stabilize low frequency variations. It's preferred to have a large number of small value capacitors in parallel rather than having a small number of large value capacitors. Every capacitor has an internal inductance in series with the specified capacitance. In addition to resonance, the capacitor will also behave like an inductor. If many capacitors are connected in parallel, total inductance will decrease while total capacitance will increase. Figure 43 shows the impedance dependence of SMD capacitors.

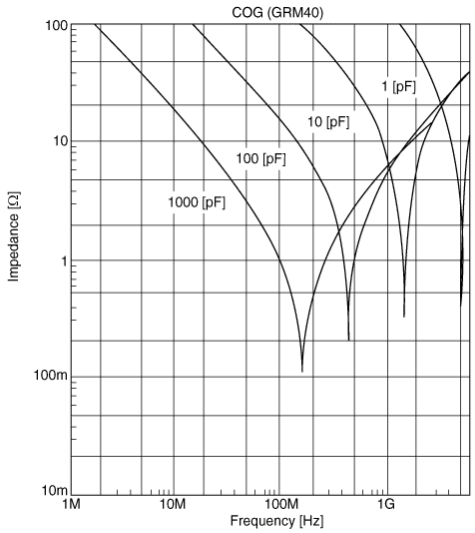


Figure 43: Impedance of 0805 size SMD capacitors vs. frequency, MuRata

If the power and ground plane are not connected by an efficient capacitor network, the power plane may act as a radiating patch antenna with respect to the ground. Furthermore, ceramic capacitors come with different dielectric materials. These materials show different temperature behavior. For industrial temperature range applications, at least a X5R quality should be selected. Y5V or Z5U types may lose almost all of their capacitance at extreme temperatures, resulting in potential system failure at low temperatures because of excessive noise

emissions from the digital part. Tantalum capacitors show good thermal stability, however, their high ESR (equivalent series resistance) limits the usable frequency range to some 100 kHz.

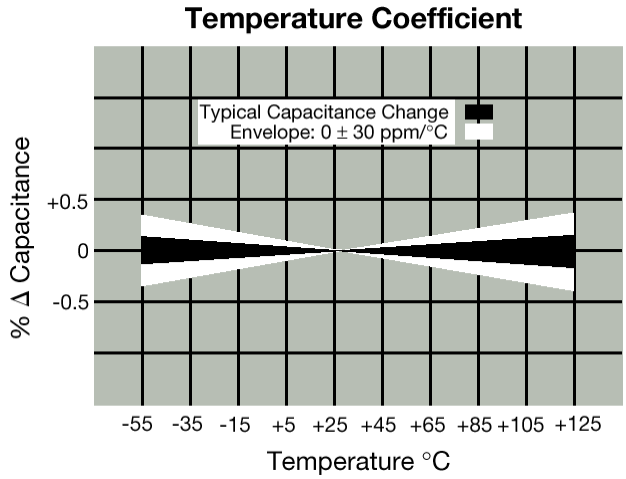


Figure 44: Temperature dependency of COG/NPO dielectric, AVX

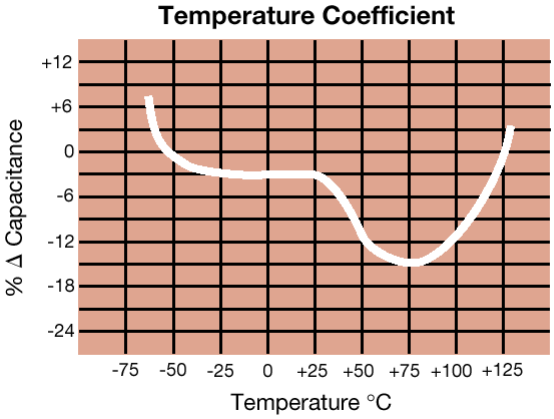


Figure 45: Temperature dependency of X7R dielectric, AVX

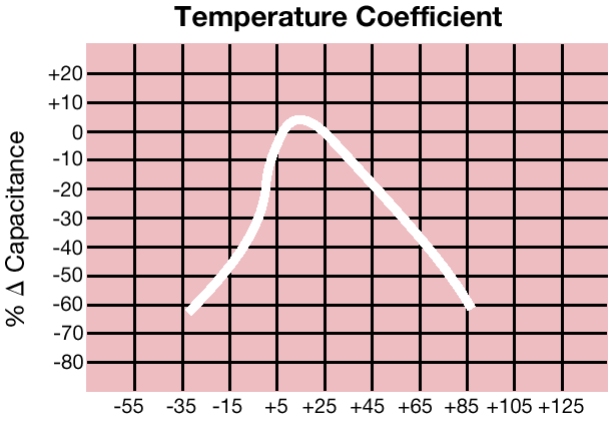


Figure 46: Temperature dependency of Y5V dielectric, AVX

D.3 Shielding

If employing the countermeasures listed in *Appendix D.2* cannot solve EMI problems, the solution may be shielding of the noise source. In the real world, shields are not perfect. The shielding effectiveness you can expect from a solid metal shield is somewhere in the order of 30-40 dB. If a thin PCB copper layer is used as a shield, these values can be even lower. Perforation of the shield will also lower its effectiveness.

Be aware of the negative effects that holes in the shield can have on shielding effectiveness. Lengthy slots might even turn a shield into a radiating slot antenna. Therefore, a proper shield has to be tightly closed and very well connected to the circuit board.

D.3.1 Feed through Capacitors

The basic concept of shielding is that a metal box will terminate all electrical fields on its surface. In practice we have the problem that we need to route some signals from inside to outside of this box.

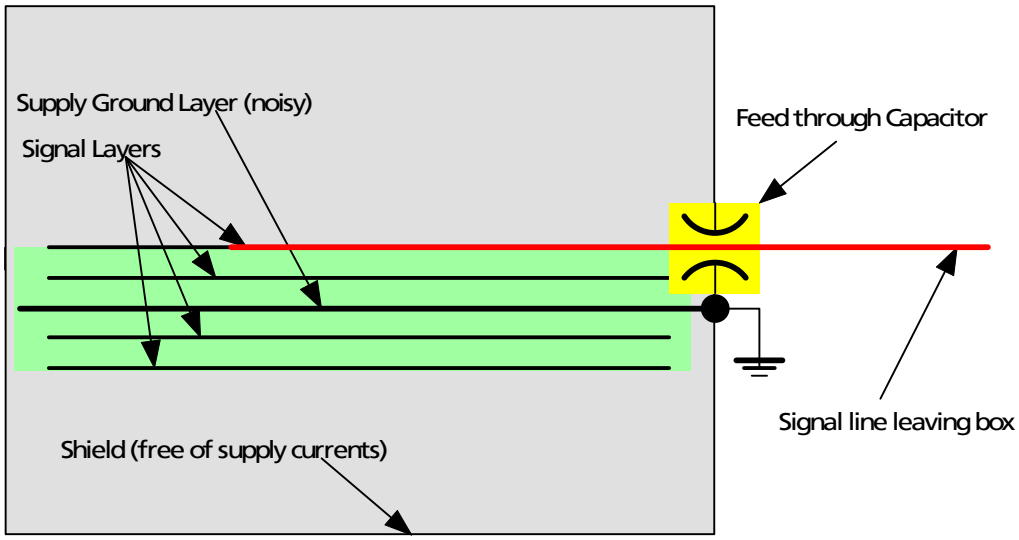


Figure 47: Ideal shielding

The proposed setup for such a system is shown in Figure 47. A feed through capacitor removes all high frequency content from the outgoing signal line. It's important to note that any conductor projecting through the shielding box is subject to picking up noise inside and re-radiating it outside, regardless of the actual signal it is intended to carry. Therefore, also DC lines (e.g. the power supply) should be filtered with feed through capacitors. When selecting feed through capacitors, it's important to choose components with appropriate frequency behavior. As with the ordinary capacitors, small value types will show better attenuation at high frequencies (see Figure 47). For the GPS/GALILEO frequency band the 470pF capacitor is the optimum choice of the Murata NFM21C series.

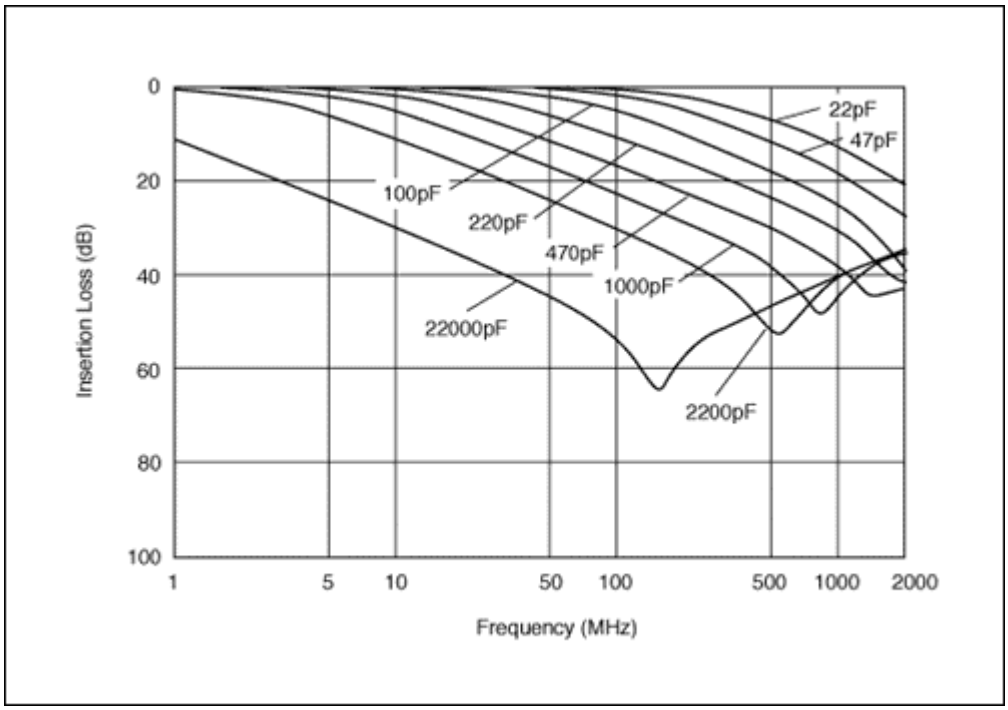


Figure 48: MuRata's NFM21C Feed Through Capacitors

Any feed through capacitor will only achieve its specified performance if it has a proper ground connection.

If the use of a special feed through capacitor is not feasible for a particular design, a simple capacitor between the signal line and shielding ground placed very close to the feed through of the signal line will also help. It has been found that a 12 pF SMD capacitor works quite well at the GPS/GALILEO frequency range. Larger capacitance values will be less efficient.

One should keep in mind that a feed through capacitor is basically a high frequency "short" between the signal line and ground. If the ground point that the capacitor is connected to is not ideal, meaning the ground connection or plane has a finite resistance, noise will be injected into the ground net. Therefore, one should try to place any feed trough capacitor far away from the most noise sensitive parts of the circuit. To emphasize this once again, one should ensure a very good ground connection for the feed through capacitor.

If there is no good ground connection available at the point of the feed through, or injection of noise into the non-ideal ground net must be avoided totally, inserting a component with a high resistance at high frequencies might be a good alternative. Ferrite beads are the components of choice if a high DC resistance cannot be accepted. Otherwise, for ordinary signal lines one could insert a 1 K series resistor, which would then form a low-pass filter together with the parasitic capacitance of the conductor trace.

See also the MuRata web page for extensive discussion on EMC countermeasures.

D.3.2 Shielding Sets of Sub-System Assembly

Yet another problem arises if multiple building blocks are combined in a single system. Figure 49 shows a possible scenario. In this case, the supply current traveling through the inductive ground connection between the two sub-systems will cause a voltage difference between the two shields of the sub-system. The shield of the other system will then act as a transmitting antenna, radiating with respect to the ground and shield of the GPS/GALILEO receiver and the attached antenna.

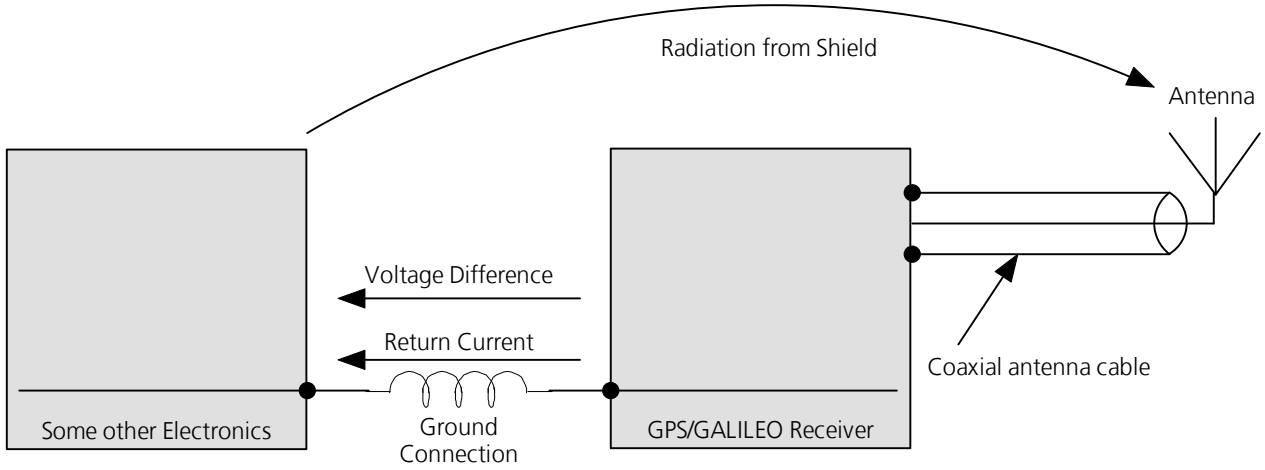


Figure 49: Two shielded sub-systems, connected by a "poor" ground

This situation can be avoided by ensuring a low inductivity ground connection between the two shields. But now, it might be difficult to control the path of the ground return currents to the power supply since the shield is probably connected to the supply ground at more than one location. The preferred solution is shown in Figure 50. Again, it is important to have a good (i.e. low inductance) interconnection between the outer shield and the shielding ground of the GPS/GALILEO receiver.

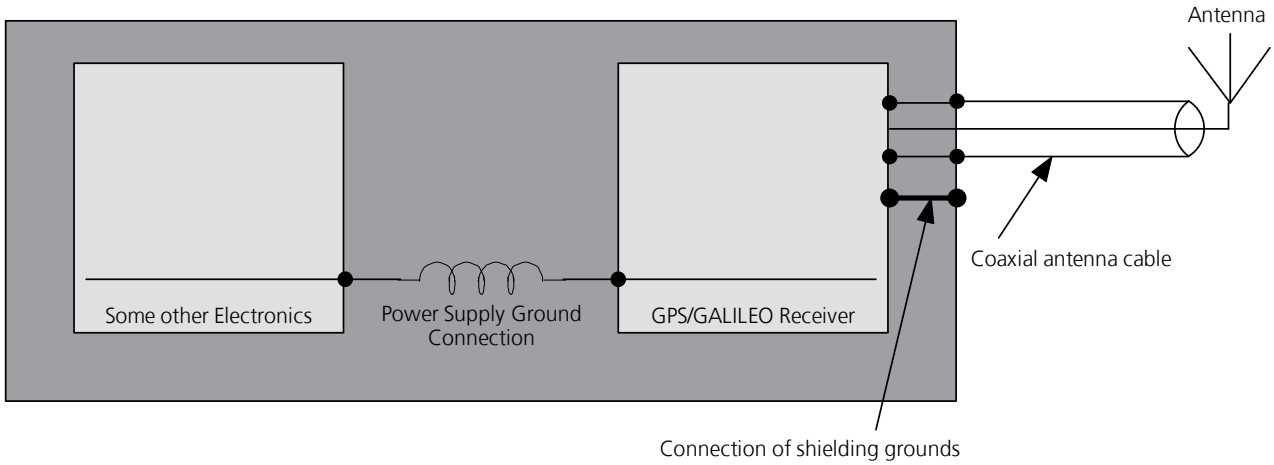


Figure 50: Proper shielding of a sub-system assembly

It is clear that the situation illustrated in Figure 50 can become complex if the component "Some other electronics" contains another wireless transmitter system with a second antenna, which is referenced to the systems shielding ground. As already pointed out, in a setup like this it is important to keep the shield free from supply currents with high frequency spectral content. If there are to be additional connections to the shielding ground, these should be of a highly inductive nature.

E Lists

E.1 List of Figures

E.2 List of Tables

F Glossary

BBR	Battery backup RAM
ESD	Electro Static Discharge
GNSS	Global Navigation Satellite System
LNA	Low Noise Amplifier
MSL	Height above Mean Sea Level or Orthometric Height
NMEA 0183	ASCII based standard data communication protocol used by GPS receivers.
PUBX	u-blox proprietary extension to the NMEA protocol
UBX	File extension for u-center log file or short form for the UBX protocol
UBX Protocol	A proprietary binary protocol used by the u-blox GPS technologies

Related Documents

[1] u-blox 5 Protocol Specification, Docu. No GPS.G5-X-07036

[2] GNSS Compendium, Doc No GPS-X-02007

[3] LEA-5 Data Sheet, Doc No GPS.G4-MS5-07026

All these documents are available on our homepage (http://www.u-blox.com).

☞ For regular updates to u-blox documentation and to receive product change notifications please register on our homepage.

Contact

For further info, please contact us:

Headquarters

u-blox AG

Zuercherstrasse 68
CH-8800 Thalwil
Switzerland

Phone: +41 44 722 74 44
Fax: +41 44 722 74 47
E-mail: info@u-blox.com

www.u-blox.com

Offices

North, Central and South America

u-blox America, Inc.

1902 Campus Commons Drive
Suite 310
Reston, VA 20191
USA

Phone: +1 (703) 483 3180
Fax: +1 (703) 483 3179
E-mail: info_us@u-blox.com

Regional Office West Coast:

8600 Lemon Ave #1
La Mesa, CA 91941
USA

Phone: +1 (619) 741 3011
Fax: +1 (619) 741 4334
E-mail: info_us@u-blox.com

Technical Support:

Phone: +1 (703) 483 3185
E-mail: support_us@u-blox.com

Europe, Middle East, Africa

u-blox AG

Zuercherstrasse 68
CH-8800 Thalwil
Switzerland

Phone: +41 44 722 74 44
Fax: +41 44 722 74 47
E-mail: info@u-blox.com

Technical Support:

Phone: +41 44 722 74 74
E-mail: support@u-blox.com

Asia, Australia, Pacific

u-blox Singapore Pte. Ltd.

435 Orchard Road
#17-01, Wisma Atria,
Singapore 238877

Phone: +65 6734 3811
Fax: +65 6736 1533
E-mail: info_ap@u-blox.com
Support: support_ap@u-blox.com

Regional Office China:

Room 716-718
No. 65 Fuxing Road
Beijing, 100036, China

Phone: +86 10 68 133 545
Fax: +86 10 68 217 890
E-mail: info_cn@u-blox.com
Support: support_cn@u-blox.com

Regional Office Japan:

22F Shibuya Mark City West,
1-12-1 Dogenzaka Shibuya-ku
Tokyo 150-0043 Japan

Phone: +81 3 4360 5343
Fax: +81 3 4360 5301
E-mail: info_jp@u-blox.com
Support: +81 3 4360 5344
support_jp@u-blox.com

Regional Office Korea:

Room 501, Gyeong Hui Building 109-18,
Samseong-Dong,
GangNam-Gu,
Seoul, Korea 135-090

Phone: +82 2 542 0861
Fax: +82 2 542 0862
E-mail: info_kr@u-blox.com
Support: support_kr@u-blox.com

Regional Office Taiwan:

Room 305
3F, #181, ZouTze Street
Neihu Dis.
Taipei, Taiwan

Phone: +886 2 2657 1090
Fax: +886 2 2657 1097
E-mail: info_tw@u-blox.com
Support: support_tw@u-blox.com