## A Vending Machine System Description in SystemC 2.0

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### Abstract

SystemC is a C++ class library and a methodology which can be used to create a system-level model, quickly simulate to validate and optimize the design, explore algorithms and provide the hardware and the software development team with an executable specification of the system. This work presents a description of a complete Vending Machine System using SystemC 2.0.

### 1. Introduction

The SystemC Class Library provides the necessary constructs to model system architecture including hardware timing, concurrency and reactive behavior that are missing in standard C++. The modeling of systems in SystemC 2.0 is made above the RTL level of abstraction, including systems that might be implemented in software or hardware or some combination of both.

In order to acquire more confidence with the SystemC specification mechanism the behavior of a complete digital system, a Vending Machine, has been described.

After Reset, the machine waits until a soft drink is requested . When a drink is selected, the machine verifies the stock for the particular soft drink. After that, the machine waits for coins. If the total paid is not enough, the machine refunds the value paid to the client. Otherwise it calculates the change and checks if the balance in the machine is enough for giving the change. If so, the machine delivers the soft drink and the change . If not, the client is notified and decides either to pay more for the drink or to receive a refund. When giving the change, the machine calculates the change value in number of coins of 50, 25, 10, 5 and 1 cents.

### 2. Related work

Several works about system level specification with SystemC have been made.

Stuart Swan[1], shows how to use SystemC 2.0 new system level modeling constructs enabling users to easily model communication and synchronization in systems and also to implement new models of computation within SystemC.

SystemC 2.0 User Guide[2], presents several complete models in SystemC and VHDL, so that the VHDL designer can compare these models and learn how to write better SystemC models.

Functional Specification for SystemC 2.0[3], describes the core language features and the elementary channels that are part of SystemC, by the specification of small examples.

Another Vending Machine control approach composed by VHDL modules can also be found, Synopsys[4].

However, none of these works, describes a complete Vending Machine System in SystemC. In this work a complete SystemC specification for a Vending Machine is presented. This description includes a Tester module which allows automatic testbench generation.

In section three we describe the design methodology used to implement the Vending Machine. In section four we describe the behavior of the Vending Machine as well each module. Finally, the section five shows different simulations of distinct situation when using the Vending Machine.

### 3. SystemC Methodology

The Vending Machine System was specified as a set of SystemC modules. The SystemC design approach offers many advantages over the traditional approach for system level design. The SystemC design methodology for hardware is shown in the Figure 1 and allows description refinement until the synthesis can be done.



This technique has a number of advantages over the current design methodology: During the design refinement specification not must be converted from a C level description to an HDL which represents a large effort. The design is slowly refined in small sections to add the necessary hardware and timing constructs to produce a good design. Using this refinement methodology, the designer can more easily implement design changes and detect bugs during refinement.

Written in a single language, the designer does not have to be an expert in multiple languages. SystemC allows modeling from the system level to RTL, if necessary.

Testbenches can be reused from the system level model to the RTL model saving conversion time. Using the same test bench also gives the designer a higher confidence at the system level and the RTL model implement the same functionality.

The SystemC approach provides higher productivity because the designer can model at a higher level. Writing at a higher level can result in smaller code that is easier to write and simulates faster than traditional modeling environments.

# 4. The Vending Machine Specification in SystemC

The Vending Machine is a synchronous system divided into four modules. The control module is a finite state machine (FSM) that sends signals for the other modules depending on the inputs or state transitions. This module also reads signals from a Tester module and sends signals to the Supply and the Display modules. The system modules are showed in Figure 2. Each module provides a specific function and was implemented separately in hierarchical approach.





Figure 2 – Diagram block

The Control module, the most important one, is the module that manage the FSM. The first state reset the controls signals preparing the machine for the new cycle and after pass for the second state. In the second state the machine wait for the an order of drink, signal takeDrink activated, then is checked what kind of drink was chosen and if it there is in the supply, case such condition was satisfied the machine pass for the next state else it keep in the same state waiting a new drink is chose. The third state calculate the value of the money inserted and when sufficient release the drink. The passage for the next state occurs when the drink is released or after some clock cycles without coin insertion. At the fourth, and finally state, is calculated and released the change, so the machine come back for he state initial. The Figure 3 is show a scheme with the states of the machine and theirs connections.



Figure 3 – Control state diagram

The Supply module controls the input and release of drinks and informs the control module if the chosen drink is available. The Display module shows programmed messages and instructions received of the Control module for the client.

Finally, The Tester module simulates all possible situations on the system operation. In this module are generated the signals that will be send for the Control module, three different situations are simulated for the Tester module their showed in the next section.

### 5. Results

The simulations results are stored in trace files that are visualized in GTKWave[5], which is a VCD format electronic waveform viewer (built using the GTK+ toolkit).

Figures 4, 5 and 6 show the simulation of Vending Machine for different situations.

Figure 4 shows a situation when the chosen drink is available and enough money was inserted.

In this simulation two coins of fifty cents are inserted (coinValue equal 50), the signal freeDrink is enabled, and finally the change is calculated and stored in the signal retCoin to be released.

Figure 5 shows a situation when there is enough money but the chosen drink is not available.

In this simulation two coins of fifty cents are inserted, but the drink chosen is not available. This feature can be observed in the signal supplyDrinkCode (0111), which indicate that the drink chosen, drinkCode (11).

Figure 6 shows a situation when the money is not enough and the coin insertion has stopped. After some cycles of clock the coins are returned.

In this simulation one coin of ten cents is inserted, coinValue equal 10, after ten clock cycles the signal hasRetCoin is enabled and the money accumulated is returned.

### 6. Conclusion

A complete implementation of Vending Machine based on a SystemC methodology was presented in this work. This example shows that SystemC is a specification mechanism that enables the description, implementation and test of simple and complex digital systems. All modules of the Vending Machine were described in SystemC including a module for generating testbenches. All system was described in 691 code lines.

More complexes examples are under development including an ATM Commuter and a MIPS microprocessor.

#### 7. Bibliography

[1] Stuart Swan, Cadence Design Systems Inc. An Introduction to System Level Modeling in SystemC 2.0, May 2001.

[2] Several collaborators of Open SystemC Initiative, SystemC 2.0 User Guide , October 2001.

[3] Several collaborators of Open SystemC Initiative, Functional Specification for SystemC 2.0, October 2001.

[4] Synopsys, VHDL Compiler Reference, <u>http://cwc.ucsd.edu/courses/billlin/ece111/lecture-notes/Synopsys-VHDL/aa.pdf</u>

[5] GTKWave, Amulet Group, <u>http://www.cs.man.ac.uk/amulet/tools/gtkwave/</u>

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# Figure 4 - Simulation 1

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Figure 5 - Simulation 2

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Figure 6 - Simulation 3